LARGE DIPIPM Ver.4

APPLICATION NOTE

PS21A7* series

MITSUBISHI ELECTRIC CORPORATION

POWER DEVICE WORKS
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CHAPTER 1 INTRODUCTION

1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

1.2 Product Line-up

Table 1-1. Line-up

<table>
<thead>
<tr>
<th>Type Name</th>
<th>IGBT Rating</th>
<th>Motor Rating (Note 1)</th>
<th>Isolation Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS21A79</td>
<td>50A/600V</td>
<td>3.7kW/220VAC</td>
<td>$V_{iso} = 2500$Vrms (Sine 60Hz, 1min All shorted pins-heat sink)</td>
</tr>
<tr>
<td>PS21A7A</td>
<td>75A/600V</td>
<td>5.5kW/220VAC</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

1.3 Functions and Features

Large DIPIPM Ver.4 is a compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which makes it easy for AC100-200V class low power motor inverter control. Fig.1-1, Fig.1-2 and Fig.1-3 show the outline photograph, internal cross-section structure and the circuit block diagram respectively.

One of the most important features of Large DIPIPM Ver.4 is that it realized higher thermal dissipation by incorporating thermal structure with high thermal conductive insulated sheet, so that the chip shrink became possible and achieved higher current rating up to 75A than previous Large DIPIPM Ver.3 series despite almost same package size.
Features:

- For P-side IGBTs
  - Drive circuit
  - High voltage level shift circuit
  - Control supply under voltage (UV) protection circuit (without fault signal output)

- For N-side IGBTs
  - Drive circuit
  - Short circuit (SC) protection circuit (by using external current detecting resistor)
  - Control supply under voltage (UV) protection circuit (with fault signal output)
  - Analog output of LVIC temperature

- Fault Signal Output
  - Corresponding to SC protection and N-side UV protection

- IGBT Drive Supply
  - Single DC15V power supply

- Control Input Interface
  - High active logic

1.4 The differences of previous series (Large DIPIPM Ver.3 PS2186X) and this series

1. Enlargement of maximum current rating to 75A
   Due to change its insulation structure from mold resin insulation to insulated thermal dissipation sheet, it became possible to decrease the thermal resistance between junction and case $R_{th(j-c)}$ substantially. So that despite almost same package size, it realized higher current rating up to 75A than previous Large DIPIPM Ver.3 series.

2. Changing the method of short circuit protection (SC)
   In the previous series the shunt resistor was inserted between N terminal and power GND line for detecting short circuit current. But the loss at the resistor escalates with increasing current rating, so high wattage type resistor is needed. In this series, the current detection method was changed to the one of detecting slight sense current divided from main current by using on-chip current sense IGBTs. So that the shunt resistor inserted to main flow path for SC protection is unnecessary. For more detail, refer Section 2.2.1.

3. Analog output function of LVIC temperature
   This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC and output it by analog signal. But the heat generated at IGBT and FWDi transfers to LVIC through the mold package and the inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)
   It is able to replace the thermistor which was set on outer heat sink with this function. For more detail, refer Section 2.2.3.

4. Terminal layout
   Because of above (2), (3) functions addition and divided N-side IGBT emitter, the terminal layout was changed from Large DIPIPM Ver.3 series.
   For more detail, refer Section 2.3.
CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Specifications

The specifications are described below by using PS21A7A (75A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS21A7A are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS21A7A

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VCC</td>
<td>Applied between P-N</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage (surge)</td>
<td>VCC(surge)</td>
<td>Applied between P-N</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>Collector-emitter voltage</td>
<td>VCES</td>
<td></td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>Each IGBT collector current</td>
<td></td>
<td></td>
<td>75</td>
<td>A</td>
</tr>
<tr>
<td>Each IGBT collector current (peak)</td>
<td>ICp</td>
<td>Tc=25°C, less than 1ms</td>
<td>150</td>
<td>A</td>
</tr>
<tr>
<td>Collector dissipation</td>
<td>Pc</td>
<td>Tc=25°C, per 1 chip</td>
<td>162</td>
<td>W</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>Tj</td>
<td>-20~+150°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Control (Protection) Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>Item</td>
</tr>
<tr>
<td>Control supply voltage</td>
</tr>
<tr>
<td>Control supply voltage</td>
</tr>
<tr>
<td>Input voltage</td>
</tr>
<tr>
<td>Fault output supply voltage</td>
</tr>
<tr>
<td>Fault output current</td>
</tr>
<tr>
<td>Current sensing input voltage</td>
</tr>
</tbody>
</table>

Total System

| Item | Symbol | Condition | Rating | Unit |
| Self protection supply voltage limit (short circuit protection capability) | VCC PROT | VCC=13.5~16.5V, Inverter part | 400 | V |
| Module case operation temperature | Tc | (Note 1) | -20~+100°C |
| Storage temperature | Tstg | | -40~+125°C |
| Isolation voltage | Viso | 50Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate | 2500 | Vrms |

Note 1: Tc measurement point (Under the UN-IGBT)

[Item explanation]

(1) VCC The maximum P-N voltage in no switching state. A voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.

(2) VCC(surge) The maximum P-N surge voltage in switching state. A snubber circuit is necessary if the voltage exceeds VCC(surge).

(3) VCES The maximum sustained collector-emitter voltage of built-in IGBT.

(4) IC The allowable DC current continuously flowing at collect electrode (@Tc=25°C)

(5) Tj The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetitive temperature variation ΔTj affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.

(6) VCC(prot) The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.

(7) Tc position Tc (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.
2.1.2 Thermal Resistance
Table 2-2 shows the thermal resistance of PS21A7A.

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to case resistance</td>
<td>$R_{th(j-c)}$</td>
<td>Inverter (per 1/6 module)</td>
<td>-</td>
<td>-</td>
<td>0.77</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>$R_{th(j-c)}$</td>
<td>FWD part (per 1/6 module)</td>
<td>-</td>
<td>-</td>
<td>1.25</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(Notes 2) Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu m$ to $+200\mu m$ on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10sec is called as transient thermal impedance which is shown in Fig.2-1. $Z_{th(j-c)}$ is the normalized value of the transient thermal impedance. $Z_{th(j-c)} = Z_{th(j-c)}/R_{th(j-c)\text{max}}$ For example, the IGBT transient thermal impedance of PS21A7A in 0.1s is $0.77 \times 0.5 = 0.39K/W$.

The transient thermal impedance isn’t used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock...)

![Fig.2-1 Typical transient thermal impedance](Image)

2.1.3 Electric Characteristics (Power Part)
Table 2-3 shows the typical static characteristics and switching characteristics of PS21A7A.

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-emitter saturation voltage</td>
<td>$V_{CE(sat)}$</td>
<td>$V_{d}=V_{BE}=15V$ £ $T_j=25^\circ C$</td>
<td>-</td>
<td>1.55</td>
<td>2.05</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN}=5V$, $I_c=75A$, $T_j=125^\circ C$</td>
<td>-</td>
<td>1.65</td>
<td>2.10</td>
<td>V</td>
</tr>
<tr>
<td>FWD forward voltage</td>
<td>$V_{EC}$</td>
<td>$V_{CE}=0V$, $I_c=75A$</td>
<td>-</td>
<td>1.70</td>
<td>2.20</td>
<td>V</td>
</tr>
<tr>
<td>Switching time</td>
<td>$t_{on}$</td>
<td>$V_{CC}=300V$, $V_{d}=V_{DB}=15V$</td>
<td>1.80</td>
<td>2.40</td>
<td>3.60</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>$I_c=75A$, $V_{IN}=0-5V$</td>
<td>-</td>
<td>0.30</td>
<td>-</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_{(on)}$</td>
<td>$T_j=125^\circ C$</td>
<td>-</td>
<td>0.40</td>
<td>0.60</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_{off}$</td>
<td>Inductive load (upper-lower arm)</td>
<td>-</td>
<td>3.40</td>
<td>4.80</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_{java}$</td>
<td>$I_{on}$</td>
<td>-</td>
<td>0.80</td>
<td>1.20</td>
<td>mA</td>
</tr>
<tr>
<td>Collector-emitter cut-off current</td>
<td>$I_{CES}$</td>
<td>$V_{CE}=V_{GES}$ £ $T_j=25^\circ C$</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_j=125^\circ C$</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>mA</td>
</tr>
</tbody>
</table>

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.
2.1.4 Electric Characteristics (Control Part)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit current</td>
<td>$I_D$</td>
<td>$V_D=V_{DS}=15V$ Total of $V_{P1}-V_{PC},V_{N1}-V_{NC}$</td>
<td>-</td>
<td>-</td>
<td>5.50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS}=5V$</td>
<td>-</td>
<td>-</td>
<td>0.55</td>
<td>mA</td>
</tr>
<tr>
<td>Fo output voltage</td>
<td>$V_{FOH}$</td>
<td>$V_{sc}=0V$, Fo terminal pull-up to 5V by 10kΩ</td>
<td>4.9</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{FOL}$</td>
<td>$V_{sc}=1V$, $I_{FO}=1mA$</td>
<td>-</td>
<td>-</td>
<td>0.95</td>
<td>V</td>
</tr>
<tr>
<td>Input current</td>
<td>$I_{IN}$</td>
<td>$VIN=5V$</td>
<td>0.7</td>
<td>1.0</td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td>Short circuit trip level (Note 3)</td>
<td>$I_{SC}$</td>
<td>$-20°C≤T_c≤100°C$, $R_s=23.2,\Omega$ (±1%), Not connecting outer shunt resistors to $NU,NV,NW$ terminals</td>
<td>127</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>Control supply under-voltage protection</td>
<td>$UV_{DBR}$</td>
<td>$T_c=100°C$ Trip level</td>
<td>10.0</td>
<td>12.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$UV_{DBR}$</td>
<td>Reset level</td>
<td>10.5</td>
<td>12.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$UV_{OC}$</td>
<td>Trip level</td>
<td>10.3</td>
<td>12.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$UV_{OC}$</td>
<td>Reset level</td>
<td>10.8</td>
<td>13.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Fault output pulse width</td>
<td>$t_{FO}$</td>
<td>$C_{PD}=22nF$ (Note 4)</td>
<td>1.6</td>
<td>2.4</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td>ON threshold voltage</td>
<td>$V_{th(on)}$</td>
<td>Applied between $U_{P1},V_{P1}-V_{PC}$</td>
<td>2.1</td>
<td>2.3</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td>OFF threshold voltage</td>
<td>$V_{th(off)}$</td>
<td>$U_{IN},V_{IN},V_{IC}$</td>
<td>0.8</td>
<td>1.4</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>Temperature output</td>
<td>$V_{OT}$</td>
<td>At LVIC temperature=85°C (Note 5)</td>
<td>3.57</td>
<td>3.63</td>
<td>3.69</td>
<td>V</td>
</tr>
</tbody>
</table>

(Note 3) Short circuit (SC) protection is functioning only for N-side IGBTs.
(Note 4) Fault signal is output when the lower arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width $t_{FO}$ depends on the capacitance value of $C_{PD}$: $t_{FO}(\text{typ})=C_{PD}/(9.1 \times 10^{6})$.[6]
(Note 5) DIPIPM don’t shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protect level that customer defined, controller (MCU) should stop the DIPIPM.

Fig.2-2 Switching time definition
Fig.2-3 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation

Fig.2-4 Typical switching waveform (PS21A7A)
Conditions : $V_{CC}=300V$, $V_{P}=V_{DS}=15V$, $T_{j}=125°C$, $I_{C}=75A$, Inductive load half-bridge circuit
2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS21A7A are given in Table 2-5. Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

Table 2-5 Recommended operating conditions of PS21A7A

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Recommended</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VCC</td>
<td>Applied between P-NU,NV,NW</td>
<td>0</td>
<td>300</td>
</tr>
<tr>
<td>Control supply voltage</td>
<td>VD</td>
<td>Applied between Vp-VPC,Vn-VNC</td>
<td>13.5</td>
<td>15.0</td>
</tr>
<tr>
<td>Control supply voltage</td>
<td>VDB</td>
<td>Applied between VUFB-VUFS,VVFB-VVFS, VWFB-VWFS</td>
<td>13.0</td>
<td>15.0</td>
</tr>
<tr>
<td>Control supply variation</td>
<td>ΔVDB</td>
<td>-1</td>
<td>+1</td>
<td>V/μs</td>
</tr>
<tr>
<td>Arm-shoot-through blocking time</td>
<td>tdead</td>
<td>For each input signal, Tc≤100°C</td>
<td>2.7</td>
<td>-</td>
</tr>
<tr>
<td>PWM input frequency</td>
<td>fPWM</td>
<td>Tc≤100°C, Tj≤125°C</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Output rms current</td>
<td>Io</td>
<td>VCC=300V, VD=15V, PF=0.8, Sinusoidal PWM, Tc≤100°C, Tj≤125°C</td>
<td>fPWM=5kHz</td>
<td>-</td>
</tr>
<tr>
<td>Output rms current</td>
<td>Io</td>
<td>VCC=300V, VD=15V, PF=0.8, Sinusoidal PWM, Tc≤100°C, Tj≤125°C</td>
<td>fPWM=15kHz</td>
<td>-</td>
</tr>
<tr>
<td>Minimum input pulse width</td>
<td>PWIN(on)</td>
<td>VCC=300V, VD=15V, PF=0.8, Sinusoidal PWM, Tc≤100°C, Tj≤125°C</td>
<td>1.3</td>
<td>-</td>
</tr>
<tr>
<td>Minimum input pulse width</td>
<td>PWIN(off)</td>
<td>200≤VCC≤350V, 13.5≤VD≤16.5V, 13.5≤VD≤18.5V, -20≤TC≤100°C, N line wiring inductance less than 10mH</td>
<td>3.0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>75≤IC≤127.5A</td>
<td>5.0</td>
<td>-</td>
</tr>
<tr>
<td>VNC variation</td>
<td>VNC</td>
<td>Potential difference between VNC-NU,NV,NW including surge voltage</td>
<td>-5.0</td>
<td>-</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>Tj</td>
<td>-20</td>
<td>+125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(Note 7) The allowable output rms current also depends on user application conditions.
(Note 8) Input signal with ON pulse width less than PWIN(on) might make no response.
(Note 9) IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).

Please refer below about delayed response.

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)

Real line: off pulse width>PWIN(off), turn on time t1
Broken line: off pulse width<PWIN(off), turn on time t2
2.1.6 Mechanical Characteristics and Ratings
The mechanical characteristics and ratings are shown in Table 2-6. Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6  Mechanical characteristics and ratings of PS21A7A

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting torque</td>
<td>Mounting screw: (M4)</td>
<td>0.98</td>
<td>–</td>
<td>1.47</td>
<td>N·m</td>
</tr>
<tr>
<td>Weight</td>
<td>–</td>
<td>46</td>
<td>–</td>
<td>100</td>
<td>g</td>
</tr>
<tr>
<td>Heat sink side flatness</td>
<td>(Note 6)</td>
<td>–50</td>
<td>–</td>
<td>100</td>
<td>μm</td>
</tr>
</tbody>
</table>

Note 6: Flatness measurement position
2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in the large DIPIPM Ver.4. The detailed information are described below.

2.2.1 Short Circuit Protection

In large DIPIPM Ver.4 series, the method of SC protection is different from current products, which detect main current by shunt resistor inserted into main current path. But this SC protection detects much smaller sense current (split at N-side IGBT) by measuring the potential of sense resistor Rs, which is connected to Vsc terminal. So high wattage type shunt resistor isn't necessary for SC protection, and the loss at shunt resistor can be reduced. (Fig.2-5)

![SC Protection Circuit Diagram](image)

*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

SC protection works by feedback the potential, which is generated by sense current flowing into the sense resistor, to CIN terminal. And when SC protection occurs, DIPIPM shuts down all N-side IGBTs hardly and outputs Fo signal. (its pulse width is set by CFO capacitor.)

To prevent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to 1.5-2.0μs because guaranteed short circuit protection capability of DIPIPM is within 2μs.

<table>
<thead>
<tr>
<th>Rs</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS21A7A</td>
<td>23.2Ω</td>
<td>127A</td>
<td>-</td>
</tr>
<tr>
<td>PS21A79</td>
<td>40.2Ω</td>
<td>85A</td>
<td>-</td>
</tr>
</tbody>
</table>

**Table 2-7 SC protection trip level**

Condition: Tj=-20°C~125°C, Not connecting outer shunt resistors to NU, NV, NW terminals

Normally, 23.2Ω and 40.2Ω (both E96 series) are recommended to PS21A7A and PS21A79 respectively. If it is necessary to change the trip level, it can be achieved by changing sense resistance. But lower resistance than these values is not permitted.

The SC protection level depends on the sense resistance and the temperature. Their characteristics vs. sense resistance for PS21A7A and PS21A79 are described as Fig.2-6 and Fig.2-7.
For sense resistor, its big fluctuation leads to big fluctuation of SC trip level. So it is necessary to select small variation in the resistance (within +/-1% is recommended).

And its wattage can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 3000:1 for PS21A7A and PS21A79. (In this case maximum sense current flows.) The estimation example for PS21A7A is described as below.

---

**Fig.2-6 Sense resistance Rs vs. SC trip level for PS21A7A**
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)

**Fig.2-7 Sense resistance Rs vs. SC trip level for PS21A79**
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)
[Estimation example]

(1) Normal operation state
   It is assumed that the maximum main current for normal operation is 150A (rated current x 2, for keeping a margin) and the sense resistance is 23.2Ω.
   In this case, the maximum sense current flows through the sense resistor is calculated as below.

\[
150A / 3000 = 50mA
\]

And the loss at the sense resistor is

\[
P = I^2 \cdot R \cdot t = (50mA)^2 \cdot 23.2\Omega \cdot 1s = 58mW
\]

(2) Short circuit state
   When short circuit occurs, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =750A) flows. So the sense current is

\[
750A / 3000 = 250mA
\]

But this current shut down within 2μs by SC protection. And the loss at the sense resistor is

\[
P = I^2 \cdot R \cdot t = (250mA)^2 \cdot 23.2\Omega \cdot 2\mu s = 0.0029mW
\]

As explained above, over 1/8W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]
   It takes more time (like as Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC’s transfer delay)

<table>
<thead>
<tr>
<th>Item</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC transfer delay time</td>
<td>0.3</td>
<td>0.5</td>
<td>1.0</td>
<td>μs</td>
</tr>
</tbody>
</table>

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and the this IC delay.

SC protection (N-side only, with external resistor and RC filter)
   a1. Normal operation: IGBT turn on and carry current.
   a2. Short circuit current is detected (SC trigger).
   a3. All N-side IGBTs' gates are hard interrupted.
   a4. All N-side IGBTs turn OFF.
   a5. Fo output with a fixed pulse width (determined by the external capacitance \( C_{FO} \)).
   a7. Input “H”: IGBT on, but during the Fo output period the IGBT will not turn on.
   a8. IGBT turns ON when L→H signal is input after Fo is reset.

N-side control input

Protection circuit state

Internal IGBT gate

Output current \( I_c \)

Sense voltage of \( R_s \)

Fault output \( F_o \)

Fig.2-8 SC protection timing chart
2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-9. Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

<table>
<thead>
<tr>
<th>Control supply voltage</th>
<th>Operating behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-4.0V (P, N)</td>
<td>Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIPIMP malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-signals to DIPIMP before the control supply coming up to 13.5V)</td>
</tr>
<tr>
<td>4.0-UV trip level (P, N)</td>
<td>UV function become active and output Fo (N-side only). Even if control signals are applied, IGBT does not work</td>
</tr>
<tr>
<td>UV trip level-13.5V(N),13.0V(P)</td>
<td>IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,</td>
</tr>
<tr>
<td>13.5-16.5V (N), 13.0-18.5V (P)</td>
<td>Recommended conditions. (Normal operation)</td>
</tr>
<tr>
<td>16.5-20.0V (N),18.5-20.0V (P)</td>
<td>IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.</td>
</tr>
<tr>
<td>20.0V- (P, N)</td>
<td>Over maximum voltage rating. The control circuit will be destroyed.</td>
</tr>
</tbody>
</table>

Ripple Voltage Limitation of Control Supply

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIPIM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

\[
dV/dt \leq +/-1V/\mu s, \ V_{ripple} \leq 2V_{p-p}
\]

N-side UV Protection Sequence

a1. Control supply voltage \( V_D \) rises: After \( V_D \) level reaches under voltage reset level \( UV_{Dr} \), the circuits start to operate when next input is applied.
a2. Normal operation: IGBT turn on and carry current.
a3. \( V_D \) level dips to under voltage trip level \( UV_{Dt} \).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo is output for the period determined by the capacitance \( C_{FO} \) but continuously during UV period.
a6. \( V_D \) level reaches \( UV_{Dr} \).
a7. Normal operation: IGBT turn on and carry current.

![Fig.2-9 Timing chart of N-side UV protection](image-url)
P-side UV Protection Sequence
b1. Control supply voltage \( V_{DB} \) rises: After \( V_{DB} \) level reaches under voltage reset level \( (UV_{DBr}) \), the circuits start to operate when next input is applied.
b2. Normal operation: IGBT turn on and carry current.
b3. \( V_{DB} \) level dips to under voltage trip level \( (UV_{DBt}) \).
b4. P-side IGBT turns OFF in spite of control input signal level, but there is no Fo signal output.
b5. \( V_{DB} \) level reaches \( UV_{DBr} \).

```
Control input
Protection circuit state
Control supply voltage \( V_{DB} \)
Output current \( Ic \)
Fault output \( Fo \)
```

Fig.2-10 Timing Chart of P-side UV protection

2.2.3 Temperature analog output

(1) Purpose of this function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)

It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was set on outer heat sink currently)

[Note]
DIPIPM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIPIPM.

(2) \( V_{OT} \) characteristics

The characteristics of \( V_{OT} \) output vs. LVIC temperature is described as Fig.2-11.
As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature: \( T_{ic} = V_{OT} \) output, case temperature: \( T_c \) (measuring point is defined on datasheet), and junction temperature: \( T_j \) depends on the system cooling condition, heat sink, control strategy, etc.

For example, the evaluation results in the case of using different size heat sink (table 2-10) are described as Fig.2-12. As the result of evaluations, it is clear that two cases have different relationships between LVIC temperature \( T_{ic} \) and case temperature \( T_c \).

So when setting the threshold temperature for protection, it is necessary to measure the relationship between them on your real system. And when setting threshold temperature \( T_{ic} \), it is important to consider the protection temperature is at \( T_c \leq 100^\circ C \) and \( T_j \leq 150^\circ C \).

Measuring each temperatures @ only 1 IGBT chip turns on (DC current, \( T_a = 25^\circ C \))

<table>
<thead>
<tr>
<th>Thermal resistance ( R_{th(f-a)} )</th>
<th>Heat sink size (L x D x H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 2.20K/W</td>
<td>100 x 88 x 40 mm</td>
</tr>
<tr>
<td>B 1.35K/W</td>
<td>200 x 88 x 40 mm</td>
</tr>
</tbody>
</table>

Table 2-10 Outer heat sink
The procedure example of setting protection temperature is described below.

Fig.2-13 indicates the example of the relationship between LVIC temperature $T_{ic}$, case temperature $T_c$, and junction temperature $T_j$, and Fig.2-14 is the relationship between $V_{OT}$ and $T_c$, which is obtained by combining Fig.2-11 and Fig.2-13.

If the protection level is set to $T_j=125^\circ\text{C}$ ($T_c=100^\circ\text{C}$), then $V_{OT}$ threshold level should be set 3.75V which is the maximum value @ $T_c=100^\circ\text{C}$ in Fig.2-14.

In this case the variation of real $T_c$ may become from 100$^\circ\text{C}$ to 115$^\circ\text{C}$. But even if the real $T_c$ will be maximum variation value 115$^\circ\text{C}$, $T_j$ becomes under 150$^\circ\text{C}$ ($125^\circ\text{C}+15^\circ\text{C}=140^\circ\text{C}<150^\circ\text{C}$).

As mentioned above, the relationship between $T_{ic}$, $T_c$, and $T_j$ depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of $V_{OT}$ vs. LVIC temperature and the thermocouple for measuring $T_j$.

(3) Inner circuit of $V_{OT}$ terminal

Inner circuit of $V_{OT}$ terminal is the output of OP amplifier circuit and is described as Fig.2-15.

If the resistor is inserted between $V_{OT}$ and $V_{NC}$ (control supply GND) terminals, then the current (calculated by $V_{OT}$ output ÷ resistance of inserted resistor) always flows as circuit current of LVIC.

The current capability of $V_{OT}$ output is described as Table 2-11.

<table>
<thead>
<tr>
<th>Source</th>
<th>1.7mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sink</td>
<td>0.1mA</td>
</tr>
</tbody>
</table>

Source : the current flow from $V_{OT}$ to outside.
Sink : the current flow from outside to $V_{OT}$.
2.3 Package Outlines

2.3.1 Outline Drawing

Fig. 2-16 Outline drawing
2.3.2 Power Chip Position

Fig. 2-17 indicates the center position of the each power chips.
(This figure is the view from laser marked side.)

![Fig. 2-17 Power chip position](image)

2.3.3 Laser Marking Position

The laser marking specification is described in Fig. 2-18.
Mitsubishi Corporation mark, Type name (A), Lot number (B), and QR code mark are marked in the upper side of module.

![Fig. 2-18 Laser marking view](image)
### 2.3.4 Terminal Description

#### Table 2-12 Terminal description

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U <em>P</em></td>
<td>U-phase P-side control input terminal</td>
</tr>
<tr>
<td>2</td>
<td>V <em>PC</em></td>
<td>U-phase P-side control supply positive terminal</td>
</tr>
<tr>
<td>3</td>
<td>V <em>P1</em></td>
<td>U-phase P-side drive supply positive terminal</td>
</tr>
<tr>
<td>4</td>
<td>V <em>UFB</em></td>
<td>U-phase P-side drive supply GND terminal</td>
</tr>
<tr>
<td>5</td>
<td>V <em>PG</em></td>
<td>U-phase P-side control input terminal</td>
</tr>
<tr>
<td>6</td>
<td>V <em>P1</em></td>
<td>V-phase P-side control supply positive terminal</td>
</tr>
<tr>
<td>7</td>
<td>V <em>VFB</em></td>
<td>V-phase P-side drive supply positive terminal</td>
</tr>
<tr>
<td>8</td>
<td>V <em>VFS</em></td>
<td>V-phase P-side drive supply GND terminal</td>
</tr>
<tr>
<td>9</td>
<td>W <em>P</em></td>
<td>W-phase P-side control input terminal</td>
</tr>
<tr>
<td>10</td>
<td>W <em>PC</em></td>
<td>P-side control supply GND terminal</td>
</tr>
<tr>
<td>11</td>
<td>W <em>P1</em></td>
<td>W-phase P-side control supply positive terminal</td>
</tr>
<tr>
<td>12</td>
<td>W <em>VFB</em></td>
<td>W-phase P-side drive supply positive terminal</td>
</tr>
<tr>
<td>13</td>
<td>W <em>VFS</em></td>
<td>W-phase P-side drive supply GND terminal</td>
</tr>
<tr>
<td>14</td>
<td>W <em>PG</em></td>
<td>Sense current detecting terminal</td>
</tr>
<tr>
<td>15</td>
<td>V <em>si</em></td>
<td>N-side control supply positive terminal</td>
</tr>
<tr>
<td>16</td>
<td>VN <em>NC</em></td>
<td>N-side control supply GND terminal</td>
</tr>
<tr>
<td>17</td>
<td>V <em>OT</em></td>
<td>LVIC temperature output terminal</td>
</tr>
<tr>
<td>18</td>
<td>CIN</td>
<td>SC trip voltage detect terminal</td>
</tr>
<tr>
<td>19</td>
<td>CFO</td>
<td>Fault pulse output width set terminal</td>
</tr>
<tr>
<td>20</td>
<td>F <em>O</em></td>
<td>Fault signal output terminal</td>
</tr>
<tr>
<td>21</td>
<td>U <em>N</em></td>
<td>U-phase N-side control input terminal</td>
</tr>
<tr>
<td>22</td>
<td>V <em>N</em></td>
<td>V-phase N-side control input terminal</td>
</tr>
<tr>
<td>23</td>
<td>W <em>N</em></td>
<td>W-phase N-side control input terminal</td>
</tr>
<tr>
<td>24</td>
<td>NW</td>
<td>W-phase N-side IGBT emitter terminal</td>
</tr>
<tr>
<td>25</td>
<td>NV</td>
<td>V-phase N-side IGBT emitter terminal</td>
</tr>
<tr>
<td>26</td>
<td>NU</td>
<td>U-phase N-side IGBT emitter terminal</td>
</tr>
<tr>
<td>27</td>
<td>W</td>
<td>W-phase output terminal</td>
</tr>
<tr>
<td>28</td>
<td>V</td>
<td>V-phase output terminal</td>
</tr>
<tr>
<td>29</td>
<td>U</td>
<td>U-phase output terminal</td>
</tr>
<tr>
<td>30</td>
<td>P</td>
<td>Inverter DC-link positive terminal</td>
</tr>
<tr>
<td>31</td>
<td></td>
<td>Internal use (Dummy pin)</td>
</tr>
</tbody>
</table>

*Don’t connect all dummy pins to any other terminals or PCB pattern. (Leave no connect)*
Table 2-13 Detailed description of input and output terminals

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
</table>
| P-side drive supply positive terminal | $V_{UFB}$ - $V_{UFS}$, $V_{WFB}$ - $V_{WFS}$ | - Drive supply terminals for P-side IGBTs.  
- By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIPIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side $V_D$ supply during ON-state of the corresponding N-side IGBT in the loop.  
- Abnormal operation might happen if the $V_D$ supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals.  
- Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction. |
| P-side drive supply GND terminal | | |
| P-side control supply terminal | $V_{PI}$, $V_{NI}$, $V_{PC}$, $V_{NC}$ | - Control supply terminals for the built-in HVIC and LVIC.  
- In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals.  
- Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation.  
- It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction. |
| N-side control supply terminal | | |
| N-side control GND terminal | | |
- Voltage input type. These terminals are internally connected to Schmitt trigger circuit.  
- The wiring of each input should be as short as possible to protect the DIPIPM from noise interference.  
- Use RC coupling in case of signal oscillation. (Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ)) |
| Sense current detect terminal | $V_{SC}$ | - The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here. |
| Short-circuit trip voltage detecting terminal | $CIN$ | - Input the potential of Vsc terminal (with sense resistor) to CIN terminal for SC protection through RC filter (for the noise immunity).  
- The time constant of RC filter is recommended to be up to 2μs. |
| Fault signal output terminal | $F_O$ | - Fault signal output terminal for N-side abnormal state (SC or UV).  
- This output is open drain type. $F_O$ signal line should be pulled up to a 5V logic supply with over 5kΩ resistor (for limiting the $F_O$ sink current $I_{F_UP}$ to 1mA.) Normally 10kΩ is recommended. |
| Fault pulse output width setting terminal | $CFO$ | - The terminal is for setting the fault pulse output width.  
- An external capacitor should be connected between this terminal and VNC.  
- When 22nF capacitor is connected, then the $F_O$ pulse width becomes 2.4ms.  
$\frac{I_{F_UP}}{CFO} = 9.1 \times 10^{-3}$ (s) |
| Inverter DC-link positive terminal | $P$ | - DC-link positive power supply terminal.  
- Internally connected to the collectors of all P-side IGBTs.  
- To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics. |
| Inverter DC-link negative terminal | $NU$, $NV$, $NW$ | - Open emitter terminal of each N-side IGBT  
- If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible. |
| Inverter power output terminal | $U$, $V$, $W$ | - Inverter output terminals for connection to inverter load (e.g. AC motor).  
- Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm. |

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.
2.4 Mounting Method
This section shows the electric spacing and mounting precautions.

2.4.1 Electric Spacing
The electric spacing specification of Large DIPIPM Ver.4 is shown in Table 2-14

Table 2-14 Minimum insulation distance

<table>
<thead>
<tr>
<th></th>
<th>Clearance (mm)</th>
<th>Creepage (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between live power terminals with high potential</td>
<td>7.1</td>
<td>7.9</td>
</tr>
<tr>
<td>Between live control terminals with high potential</td>
<td>3.3</td>
<td>5.6</td>
</tr>
<tr>
<td>Between terminals and heat sink</td>
<td>3.7</td>
<td>5.6</td>
</tr>
</tbody>
</table>

2.4.2 Mounting Method and Precautions
When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the device. The recommended fastening procedure is shown in Fig.2-19. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.

![Fig.2-19 Recommended screw fastening order](image)

Table 2-15. Mounting torque and heat sink flatness specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting torque</td>
<td>Recommended 1.18N·m, Screw : M4</td>
<td>0.98</td>
<td>-</td>
<td>1.47</td>
<td>N·m</td>
</tr>
<tr>
<td>Flatness of outer heat sink</td>
<td>Refer Fig.2-20</td>
<td>-50</td>
<td>-</td>
<td>+100</td>
<td>μm</td>
</tr>
</tbody>
</table>

![Fig.2-20 Measurement point of heat sink flatness](image)

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12. Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).
2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in table 2-16 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-16 Reliability test specification

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soldering Thermostability</td>
<td>260±5°C, 10±1s</td>
</tr>
</tbody>
</table>

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample : Large DIPIPM Ver.4

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe.
  (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

![Heating and measuring point](image1)

![Temperature alteration of the terminal root](image2)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.
CHAPTER 3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance
This chapter states usage and interface circuit design hints.

3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics
Note: the capacitance also depends on the PWM control strategy of the application system
C2: 0.22μF ceramic capacitor with good temperature, frequency and DC bias characteristics
C3: 0.1μF 0.22μF Film capacitor (for snubber)
D1: Bootstrap diode. High speed type with VRRM > 600V, trr: up to 100ns
D2: Zener diode 24V/1W for surge absorber

Fig. 3-1 Application System block diagram
3.1.2 Interface Circuit (Direct Coupling Interface example)

Fig.3-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly from a controller (MCU or DSP).

![Diagram](image)

**Fig.3-2 Interface circuit example (Direct coupling)**

**Note:**

1. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

2. To prevent surge destruction, the wiring between the smoothing capacitor and the P-N1 terminals should be as short as possible. Generally inserting a 0.1μ~0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

3. The time constant R1C4 of RC filter for preventing the protection circuit malfunction should be selected in the range of 1.5μ~2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C4

4. All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2 : good temperature, frequency and DC bias characteristic ceramic type are recommended.)

5. It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.

6. To prevent erroneous SC protection, the wiring from VSC terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.

7. For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 1/8W is recommended, but it is necessary to evaluate in your real system finally.

8. To prevent erroneous operation, the wiring of A, B, C should be as short as possible.

9. Fo output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits Fo sink current Ifo, under 1mA. In the case pull up to 5V supply, over R2=5.1kΩ is needed. (10kΩ is recommended.)

10. Error signal output width (tFo) can be set by the capacitor connected to CFO terminal. tFo (typ.) =CFO / 9.1x 10^-6 (s)

11. High voltage (Vbus =600V or more) and fast recovery type (trr<less than 100ns or less) diode D2 should be used in the bootstrap circuit.

12. Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be patterned as short as possible. When inserting RC filter, make sure the input signal level meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

Fig. 3-3 Interface circuit example with opto-coupler

Note:

1) High speed (high CMR) opto-coupler is recommended.
2) Fo terminal sink current is max. 1mA. A buffer circuit is necessary to drive an opto-coupler.
3.1.4 Circuits of Signal Input terminals and Fo Terminal

Large DIPIPM Ver.4 is high-active input logic. A 3.3kΩ(min) pull-down resistor is built-in each input circuit of the DIPIPM as shown in Fig.3-7, so external pull-down resistor is not needed.

![DIPIPM Internal Structure Diagram](image)

**Table 3-1** Input threshold voltage ratings (Tj=25°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-on threshold voltage</td>
<td>Vth(on)</td>
<td>U_p, V_p, W_p, V_pc</td>
<td>2.1</td>
<td>2.3</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td>Turn-off threshold voltage</td>
<td>Vth(off)</td>
<td>U_n, V_n, W_n, V_nc</td>
<td>0.8</td>
<td>1.4</td>
<td>2.1</td>
<td>V</td>
</tr>
</tbody>
</table>

The wiring of each input should be patterned as short as possible. And if the pattern is long and the noise is imposed on the pattern, it may be effective to insert RC filter.

![Control Input Connection Diagram](image)

Note: The RC coupling (parts shown in the dotted line) at each input depends on user’s PWM control strategy and the wiring impedance of the printed circuit board.

The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.
There are limits for the minimum input pulse width in the DIPIPIM. The DIPIPIM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Please refer Table 3-2)

Table 3-2 Allowable minimum input pulse width

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Condition</th>
<th>PN</th>
<th>Min. value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>On</td>
<td>PWIN(on)</td>
<td></td>
<td>PS21A79</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PS21A7A</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>Off</td>
<td>PWIN(off)</td>
<td>200 ≤ V_C ≤ 350 V, 13.5 ≤ V_D ≤ 16.5 V, 13.5 ≤ V_DB ≤ 18.5 V, -20 ≤ T_C ≤ 100 °C, N line wiring inductance less than 10 nH</td>
<td>Up to rated current</td>
<td>PS21A79</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PS21A7A</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>From rated current to 1.7x rated current</td>
<td>PS21A79</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PS21A7A</td>
<td>5.0</td>
</tr>
</tbody>
</table>

*) Input signal with ON pulse width less than PWIN(on) might make no response.
IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).
Please refer Fig.3-6 about delayed response.

![Diagram](image)

Real line···off pulse width>PWIN(off); turn on time t1
Broken line···off pulse width<PWIN(off); turn on time t2

Fig.3-6 Delayed Response with shorter input off (P-side only)
(2) Internal Circuit of Fo Terminal

Fo terminal is an open drain type, it should be pulled up to control supply (e.g. 5V) as shown in Fig.3-5. Fig.3-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. (\( I_{\text{Fo}} \) can be calculated from \( I_{\text{Fo}} = \frac{\text{control supply voltage}}{\text{pull up resistance}} \) approximately.) If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-3  Electric characteristics of Fo terminal

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault output voltage</td>
<td>( V_{\text{FOH}} )</td>
<td>( V_{\text{SC}}=0\text{V}, Fo=10\text{k}\Omega, 5\text{V pulled-up} )</td>
<td>4.9</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{FOL}} )</td>
<td>( V_{\text{SC}}=1\text{V}, Fo=1\text{mA} )</td>
<td>-</td>
<td>-</td>
<td>0.95</td>
<td>V</td>
</tr>
</tbody>
</table>

![Fig.3-7  Fo terminal typical V-I characteristics (\( V_{\text{D}}=15\text{V}, T_{j}=25^\circ\text{C} \))](image)

3.1.5 Snubber Circuit

In order to prevent DIPIPM from the surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. Also, a 0.1\( \mu \text{F}-0.22\mu \text{F}/630\text{V} \) snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.
3.1.6 Influence of wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

![Diagram](image)

**Fig. 3-9 External protection circuit**

(1) **Influence of the part-A wiring**

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) **Influence of the part-B wiring pattern**

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will drop down and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, VNC terminals as close as possible.

(3) **Influence of the part-D wiring pattern**

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.
3.1.7 Precaution for wiring on PCB

**Case example of trouble due to PCB pattern**

<table>
<thead>
<tr>
<th>Case example</th>
<th>Matter of trouble</th>
</tr>
</thead>
</table>
| 1 | •Control GND pattern overlaps power GND pattern. The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.  
•Ground loop pattern is existing. Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs. |
| 2 | •Long pattern between NU, NV, NW terminals and N1 Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below.  
•HVIC malfunction by VS voltage (output terminal potential) decreasing excessively.  
•LVIC surge destruction |
| 3 | Capacitors or zener diodes are nothing or located far from the terminals. IC surge destruction or malfunction occurs. |
| 4 | The input lines are located parallel and close to the floating supply lines for P-side drive. The cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then since the incorrect signals are input to DIPIPM, the arm short circuit might occur. |

---

**Fig.3-10 Precaution for wiring on PCB**

- **1.** It is recommended to connect control GND and power GND at only a point. (Not connect common broad pattern)
- **2.** NU, NV, NW should be connected each other as close to the terminals as possible.
- **3.** Capacitor and Zener diode should be located at near terminals
- **4.** These wire potentials fluctuate between Vcc and GND potential at switching, so it may cause malfunction if wires for control (e.g. control input Vin, control supply) are located near by or cross these wires. Particularly pay attention when using multi layered PCB. It is recommended to locate wires for control as far from these wires as possible, and pass under the resistor, diode or jumper if need to cross.
3.1.8 SOA of DIPIPM

The following describes the SOA (Safety Operating Area) of DIPIPM.

- **V\textsubscript{CES}**: Maximum rating of IGBT collector-emitter voltage
- **V\textsubscript{CC}**: Supply voltage applied on P-N terminals
- **V\textsubscript{CC(surge)}**: The total amount of V\textsubscript{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.
- **V\textsubscript{CC(prot)}**: DC-link voltage that DIPIPM can protect itself.

\[ V_{\text{CE}=0}, I_C=0 \leq V_{\text{CC}} \leq V_{\text{CC(surge)}} \]

\[ V_{\text{CC(prot)}} \leq V_{\text{CC(surge)}} \leq V_{\text{CC}} \]

In Case of switching

\( V_{\text{CES}} \) represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from \( V_{\text{CES}} \) is \( V_{\text{CC(surge)}} \), that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from \( V_{\text{CC(surge)}} \) derives \( V_{\text{CC}} \), that is 450V.

In Case of Short-circuit

\( V_{\text{CES}} \) represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductor from \( V_{\text{CES}} \) is \( V_{\text{CC(surge)}} \), that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from \( V_{\text{CC(surge)}} \) derives \( V_{\text{CC}} \), that is, 400V.

3.1.9 SCSOA

Fig.3-13 and Fig.3-14 show the typical SCSOA performance curves of PS21A7A and PS21A79.

Conditions: \( V_{\text{CC}}=400\text{V}, T_j=125^\circ\text{C} \) at initial state, \( V_{\text{CC(surge)}}\leq500\text{V(surge included)} \), non-repetitive, 2m load.

The DIPIPM can shutdown safely an SC current that is about 10 times of its current rating under the conditions only if the IGBT conducting period is less than 4.5\( \mu \text{sec} \).

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.
Input pulse width [μs]

Max Saturation Current≈520A
@VD=16.5V

CSTBT SC operation area

VD=18.5V
VD=16.5V
VD=15V

Fig.3-14 PS21A79 typical SC SOA curve
3.1.10 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-15 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj). (The curve is a regression curve based on 3 points of ΔTj=46, 88, 98°C with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)
3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- **Scope**
  The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- **Assumptions**
  1. PWM controlled VVVF inverter with sinusoidal output;
  2. PWM signals are generated by the comparison of sine waveform and triangular waveform.
  3. Duty amplitude of PWM signals varies between \( \frac{1-D}{2} \sim \frac{1+D}{2} \% \) (D: modulation depth).
  4. Output current various with Icp-sinx and it does not include ripple.
  5. Power factor of load output current is cos\( \theta \), ideal inductive load is used for switching.

- **Expressions Derivation**
  PWM signal duty is a function of phase angle \( x \) as \( \frac{1+D\times\sin x}{2} \), which is equivalent to the output voltage variation. From the power factor cos\( \theta \), the output current and its corresponding PWM duty at any phase angle \( x \) can be obtained as below:

  \[
  \text{Output current} = Icp \times \sin x \\
  \text{PWM Duty} = \frac{1+D\times\sin(x + \theta)}{2}
  \]

  Then, \( V_{CE(sat)} \) and \( V_{EC} \) at the phase \( x \) can be calculated by using a linear approximation:

  \[
  V_{ce(sat)} = V_{ce(sat)}(@ Icp \times \sin x) \\
  V_{ec} = (-1) \times V_{ec}(@ Ic)p(= Icp) \times \sin x
  \]

  Thus, the static loss of IGBT is given by:

  \[
  \frac{1}{2\pi} \int_{0}^{\pi} (Icp \times \sin x) \times V_{ce(sat)}(@ Icp \times \sin x) \times \frac{1+D\sin(x + \theta)}{2} \times dx
  \]

  Similarly, the static loss of free-wheeling diode is given by:

  \[
  \frac{1}{2\pi} \int_{0}^{2\pi} ((-1) \times Icp \times \sin x)(-(1) \times V_{ec}(@ Icp \times \sin x) \times \frac{1+D\sin(x + \theta)}{2} \times dx
  \]

  On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

  \[
  \frac{1}{2\pi} \int_{0}^{\pi} (P_{sw(on)}(@ Icp \times \sin x) + P_{sw(off)}(@ Icp \times \sin x)) \times f_c \times dx
  \]
FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-16, and its dynamic loss can be calculated by the following expression:

\[ P_{SW} = \frac{I_{rr} \times V_{cc} \times t_{rr}}{4} \]

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

\[ \frac{1}{2} \int_{0}^{\pi} I_{rr}(I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(I_{cp} \times \sin x) \times f_c \cdot dx \]

\[ = \frac{1}{8} \int_{0}^{\rho} I_{rr}(I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(I_{cp} \times \sin x) \times f_c \cdot dx \]

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, \( V_{CE(sat)} \), \( V_{EC} \), and \( P_{sw} \) corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - \( V_{CE(sat)}, V_{EC} \) and \( P_{sw(on, off)} \) should be the values at \( T_j=125°C \).
Fig. 3-17 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results:

- Conditions: 
  - $V_{CC}=300V$, 
  - $V_D=V_{DB}=15V$, 
  - $V_{CE(sat)}=\text{Typ.}$, 
  - $P.F=0.8$, 
  - Switching loss=Typ., 
  - $T_j=125^\circ C$, $T_c=100^\circ C$, $R_{th(j-c)}=\text{Max.}$, 
  - 3-phase PWM modulation, 
  - 60Hz sine waveform output

Fig. 3-17 Effective current-carrier frequency characteristic

Fig. 3-17 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition ($T_c=100^\circ C$ and $T_j=125^\circ C$). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided by Mitsubishi electric on its web site (URL: http://www.mitsubishichips.com/).
3.3 Noise Withstand Capability

3.3.1 Evaluation Circuit
DIPiPM have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-18. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

![Noise withstand capability evaluation circuit](image)

**Fig.3-18 Noise withstand capability evaluation circuit**

**Note:**
- C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers
- 15V single power supply, Test is performed with IM

**Test conditions**
- VCC=300V, VD=15V, Ta=25°C, no load
- Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width \(t_w=0.05-1\mu s\), input in random.

3.3.2 Countermeasures and Precautions
DIPiPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPiPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

![Example of countermeasures](image)

**Fig.3-19 Example of countermeasures**

- Insert the RC filter
- Increase the capacitance of C2 and locate it as close to the terminal as possible
- Increase the capacitance of C4 with keeping the same time constant \(R_1\cdot C_4\), and locate the C4 as close to the terminal as possible.
3.3.3 Static Electricity Withstand Capability

DIPIPM has been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-20 and Fig.3-21. The results (typical data) are described in Table 3-4.

**Fig.3-20** $V_{N1}$ terminal Surge Test circuit

| **Fig.3-21** $V_{P1}$ terminal Surge Test circuit |

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage.

(Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

Table 3-4 Typical ESD capability for PS21A7A and PS21A79

<table>
<thead>
<tr>
<th>Control terminal part</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Terminals</strong></td>
</tr>
<tr>
<td>UP, VP, WP-V&lt;sub&gt;NC&lt;/sub&gt;</td>
</tr>
<tr>
<td>$V_{P1}$ - $V_{NC}$</td>
</tr>
<tr>
<td>$V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$,$V_{WFB}$-$V_{WFS}$</td>
</tr>
<tr>
<td>UN, VN, WN-$V_{NC}$</td>
</tr>
<tr>
<td>$V_{N1}$-$V_{NC}$</td>
</tr>
<tr>
<td>CIN-$V_{NC}$</td>
</tr>
<tr>
<td>FO-$V_{NC}$</td>
</tr>
<tr>
<td>CFO-$V_{NC}$</td>
</tr>
<tr>
<td>VOT-$V_{NC}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power terminal part for PS21A7A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Terminals</strong></td>
</tr>
<tr>
<td>$V_{SC}$-$V_{NC}$*</td>
</tr>
<tr>
<td>$P$-$NU$, $NV$, $NW$</td>
</tr>
<tr>
<td>$U$-$NU$, $V$-$NV$, $W$-$NW$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power terminal part for PS21A79</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Terminals</strong></td>
</tr>
<tr>
<td>$V_{SC}$-$V_{NC}$*</td>
</tr>
<tr>
<td>$P$-$NU$, $NV$, $NW$</td>
</tr>
<tr>
<td>$U$-$NU$, $V$-$NV$, $W$-$NW$</td>
</tr>
</tbody>
</table>

* $V_{SC}$ terminal (IGBT sense) is connected to the power chip inside the module.
CHAPTER 4 KEY PARAMETERS SELECTING GUIDANCE

4.1 Single Supply Drive Scheme

4.1.1 Bootstrap Capacitor Initial Charging

By using bootstrap circuit, conventional three isolated 15V power supply for P-side three IGBT drive can be eliminated. The initial charge of the bootstrap capacitors is necessary to start-up the inverter. Fig.4-2 shows the charge mechanism. The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.

For reference, the charging time for the bootstrap circuit with a 100μF capacitor and 50Ω current limiting resistor is about 5msec.

4.1.2 Charging and Discharging of the Bootstrap Capacitor During Inverter Operation

(1) Charging operation Timing Chart of Bootstrap Capacitor (C1)

Sequence (1-1) : IGBT2 ON (Fig.4-3)

When IGBT2 is in ON state, charging voltage on C1 (\(V_{C(1)}\)) is calculated by

\[
V_{C(1)} = V_{CC} - V_{F1} - V_{sat2} \cdot I_0 \cdot R_1 \quad \text{(Transient state)}
\]

\[
V_{C(1)} = V_{CC} \quad \text{(Steady state)}
\]

where \(V_{CC}\) is the charging supply voltage, \(V_{F1}\) the forward voltage drop of diode D1, \(V_{sat2}\) the saturation voltage of IGBT2, \(I_0\) the charging current, and \(R_1\) the inrush current limitation resistance.

Then, IGBT2 is turned off. Motor current will flow through the free-wheel path of FWDi1. Once the electric potential of VS rises near to that of P, the charging to C1 is stopped.

When IGBT1 is in ON state, the voltage of C1 gradually declines from the potential \(V_{C(1)}\) due to the current consumed by the drive circuit.
Sequence (1-2): IGBT2 OFF and FWDi2 ON (Fig.4-4)
When IGBT2 is OFF and FWDi2 is ON, the voltage on C1 (V_{C(2)}) is calculated by:
\[ V_{C(2)} = V_{CC} - V_{F1} + V_{EC2} \]
where \( V_{EC2} \) denotes the forward voltage drop of FWDi2.

When both IGBT2 and IGBT1 are OFF, the regenerative current flows continuously through the free-wheel path of FWDi2. Therefore the potential of VS drops to -\( V_{EC2} \), then C1 is recharged to restore the declined potential. When IGBT1 is turned ON, the potential of VS rises to that of P, the charge to C1 stops and the voltage on C1 gradually declines from the potential \( V_{C(2)} \) due to the current consumed by the drive circuit.
Design example of Bootstrap circuit

- **Selecting bootstrap capacitor**
  Suppose $\Delta V_D=1V$, the maximum ON pulse width $T_1$ of P-side IGBT is 5msec, and $I_{DB}$ is 0.55mA(Max. rating), then
  \[
  C = \frac{I_{DB} \times T_1}{\Delta V_D} = 2.75 \times 10^{-6}
  \]
  the calculated bootstrap capacitance is $2.75\mu F$. By taking consideration of dispersion and reliability, the capacitance is generally selected as large as 2~3 times of the calculated one, for example, $10\mu F$ or above for this case is suitable.

- **Selecting bootstrap resistor**
  Suppose the bootstrap capacitance is $10\mu F$, $V_D=15V$, $V_{DB}=14V$, and the minimum ON pulse width $t_0$ of N-side IGBT (or the minimum OFF pulse width $t_0$ of upper-side IGBT) is $20\mu s$, then to recover $V_{DB}$ to 15V during this period, the bootstrap resistance should be
  \[
  R = \frac{(V_D-V_{DB}) \times t_0}{C \times \Delta V_D} = 2
  \]
  This means a $2\Omega$ resistor is suitable.

**Note:**
(1) In the case of the control for DCBLM or 2-phase modulation for IM (Induction Motor), there will be a long ON time period on the P-side IGBT, please pay attention to the bootstrap supply voltage drop.
(2) The above result is only a calculation example. It is recommended to design a system by taking consideration of the actual control pattern and lifetime of components.

For reference, Fig.4-6 and 4-7 are the circuit current $I_{DB}$ for P-side IGBT driving supply ($V_{DB}$) vs. carrier frequency characteristics (@ $V_D=V_{DB}=15V$, $T_j=125^\circ C$, IGBT ON Duty=10, 30, 50, 70, 90%)
Selecting bootstrap diode
The bootstrap diode with blocking voltage over 600V is recommended. In DIPIPM, the maximum rating of power supply is 450V. The actual voltage applied on the diode is 500V by adding a surge voltage of about 50V. Furthermore, if considering 100V for the margin, 600V class diode is necessary. The diode is also highly recommended to be with fast recovery characteristics (recovery time less than 100nsec).

Noise filter for control supply
It is recommended to insert a film type or ceramic type noise filter with 0.22-2μF to the control supply terminals (V_P1-V_NC, V_N1-V_NC, V_UFB-V_UFS, V_VFB-V_VFS, V_WFB-V_WFS). The smaller the supply parasitic impedance is, the smaller a feasible noise filter capacitance can be. The supply circuit should be such designed that the noise fluctuation is less than +/-1V/μs, and the ripple voltage is less than +/-2V.

Reference:
There are two kinds of control supply in general use. The first one is DC-DC converter (3-terminal regulator), of which input DC supply comes from AC-transformer. The other is DC-DC converter (switching regulator), of which input DC supply is generated by a SMPS.

Note:
After bootstrap capacitor voltage has been fully charged, input one pulse in the P-side input signals to reset internal IC state before starting formal PWM.
CHAPTER5 PACKAGE HANDLING

5.1 Packaging Specification

Quantity:
6pcs per 1 tube

Total amount in one box (max):
Tube Quantity: 5 × 6=30pcs
IPM Quantity: 30 × 6=180pcs

Weight (max):
About 46g per 1pcs
About 380g per 1tube
About 13kg per 1box

Fig.5-1 Packaging Specification
### 5.2 Handling Precautions

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| **Transportation**        | · Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged.  
· Throwing or dropping the packaging boxes might cause the devices to be damaged.  
· Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day. |
| **Storage**               | · We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above. |
| **Long storage**          | · When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior. |
| **Surroundings**          | · Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems. |
| **Flame resistance**      | · The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable. |
| **Static electricity**    | · ICS and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. |

(1) **Precautions against the device destruction caused by the ESD**

The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.

* Containers that charge static electricity easily should not be used for transit and for storage.  
* Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands.  
* Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands.  
* During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats.  
* When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board.  
* If using a soldering iron, earth its tip.  

(2) **Notice when the control terminals are open**

* When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.  
* Short the terminals before taking a module off.
Keep safety first in your circuit designs!

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## Appendix

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