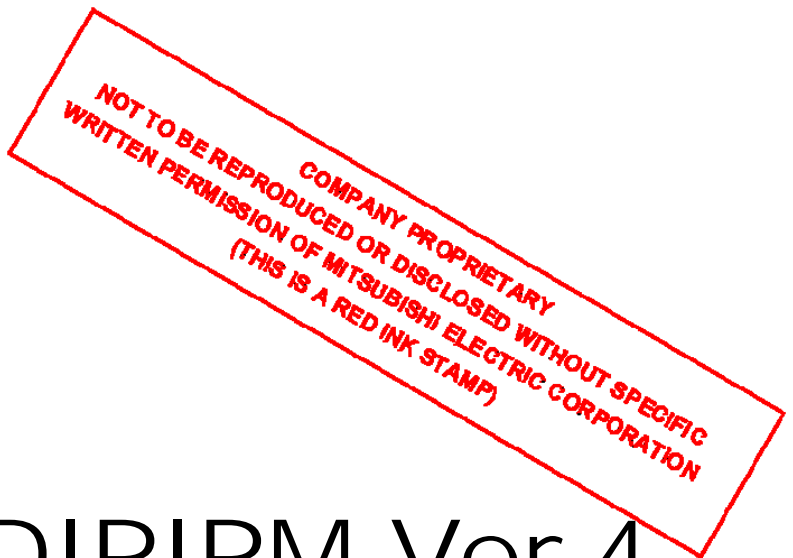




Application Note	Prep.	<i>T.Nagahara M.Sakai,Shang,T.Nakano</i>	Rev.			
	Apr.	<i>T.Iwagami 12-Feb-'09</i>				



LARGE DIIPM Ver.4

APPLICATION NOTE

PS21A7* series

MITSUBISHI ELECTRIC CORPORATION
POWER DEVICE WORKS

DIIPM	DPH-6414e	APPLICATION NOTE
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CHAPTER1 INTRODUCTION

1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

1.2 Product Line-up

Table 1-1. Line-up

Type Name	IGBT Rating	Motor Rating ^(Note 1)	Isolation Voltage
PS21A79	50A/600V	3.7kW/220V _{AC}	V _{iso} = 2500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS21A7A	75A/600V	5.5kW/220V _{AC}	

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

1.3 Functions and Features

Large DIIPM Ver.4 is a compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which makes it easy for AC100-200V class low power motor inverter control. Fig.1-1, Fig.1-2 and Fig.1-3 show the outline photograph, internal cross-section structure and the circuit block diagram respectively.

One of the most important features of Large DIIPM Ver.4 is that it realized higher thermal dissipation by incorporating thermal structure with high thermal conductive insulated sheet, so that the chip shrink became possible and achieved higher current rating up to 75A than previous Large DIIPM Ver.3 series despite almost same package size .

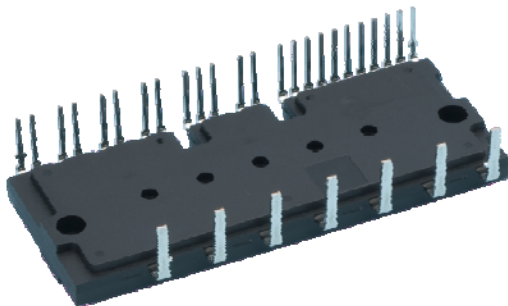


Fig.1-1 Package photograph

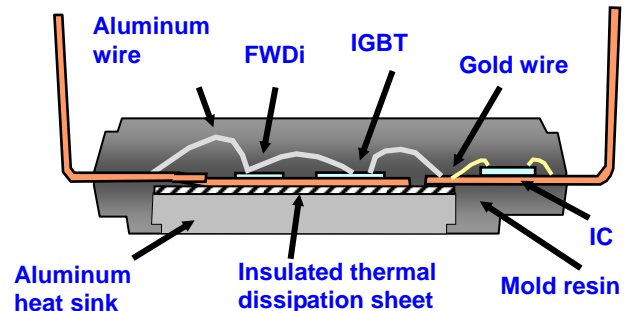


Fig.1-2 Internal cross-section structure

CHAPTER2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Specifications

The specifications are described below by using PS21A7A (75A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS21A7A are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS21A7A

Maximum Ratings (Tj=25°C, unless otherwise noted):

Inverter Part:

Item	Symbol	Condition	Rating	Unit	
Supply voltage	V _{CC}	Applied between P-NU,NV,NW	450	V	(1)
Supply voltage (surge)	V _{CC(surge)}	Applied between P-NU,NV,NW	500	V	(2)
Collector-emitter voltage	V _{CES}		600	V	(3)
Each IGBT collector current	±I _C	Tc=25°C	75	A	(4)
Each IGBT collector current (peak)	±I _{CP}	Tc=25°C, less than 1ms	150	A	
Collector dissipation	P _C	Tc=25°C, per 1 chip	162	W	
Junction temperature	T _J		-20~+150	°C	(5)

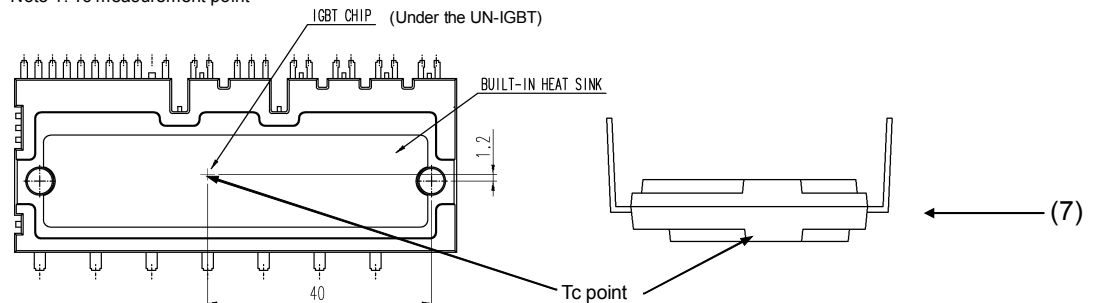
Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V _D	Applied between V _{P1} -V _{PC} , V _{N1} -V _{NC}	20	V
Control supply voltage	V _{DB}	Applied between V _{UFB} -V _{UFS} , V _{VFB} -V _{VES} , V _{WFB} -V _{WFS}	20	V
Input voltage	V _{IN}	Applied between U _P , V _P , W _P -V _{PC} , U _N , V _N , W _N -V _{NC}	-0.5~V _D +0.5	V
Fault output supply voltage	V _{FO}	Applied between Fo-V _{NC}	-0.5~V _D +0.5	V
Fault output current	I _{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V _{SC}	Applied between CIN-V _{NC}	-0.5~V _D +0.5	V

Total System

Item	Symbol	Condition	Rating	Unit	
Self protection supply voltage limit (short circuit protection capability)	V _{CC(prot)}	V _D =13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	400	V	(6)
Module case operation temperature	T _c	(Note 1)	-20~+100	°C	
Storage temperature	T _{stg}		-40~+125	°C	
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	Vrms	

Note 1: Tc measurement point



[Item explanation]

- (1) V_{CC} The maximum P-N voltage in no switching state. A voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.
- (2) V_{CC(surge)} The maximum P-N surge voltage in switching state. A snubber circuit is necessary if the voltage exceeds V_{CC(surge)}.
- (3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT.
- (4) ±I_C The allowable DC current continuously flowing at collect electrode (@Tc=25°C)
- (5) Tj The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetive temperature variation ΔTj affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.
- (6) V_{CC(prot)} The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.
- (7) Tc position Tc (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance of PS21A7A.

Table 2-2. Thermal resistance of PS21A7A

Thermal Resistance :

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	-	-	0.77	°C / W
	$R_{th(j-c)F}$	Inverter FWD part (per 1/6 module)	-	-	1.25	

(Note 2) Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10sec is called as transient thermal impedance which is shown in Fig.2-1. $Z_{th(j-c)}^*$ is the normalized value of the transient thermal impedance. ($Z_{th(j-c)}^* = Z_{th(j-c)} / R_{th(j-c)max}$) For example, the IGBT transient thermal impedance of PS21A7A in 0.1s is $0.77 \times 0.5 = 0.39K/W$.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock···)

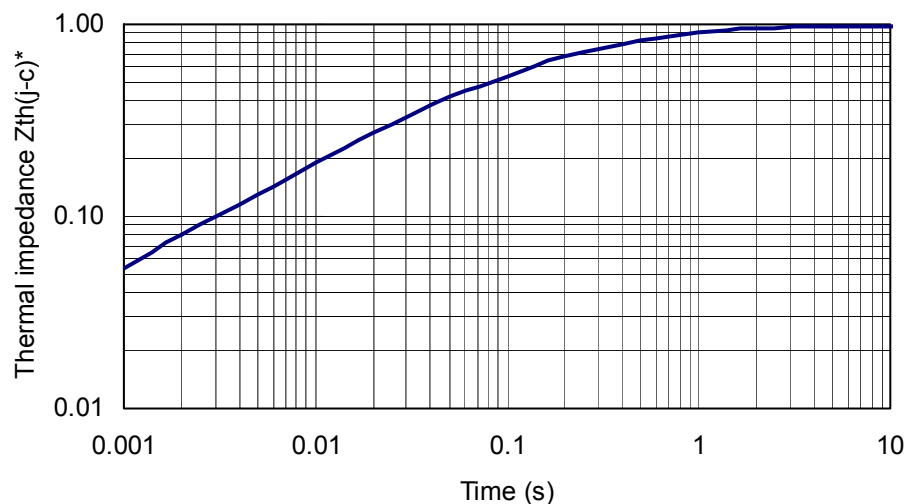


Fig.2-1 Typical transient thermal impedance

2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics of PS21A7A.

Table 2-3. Static characteristics and switching characteristics of PS21A7A

Inverter Part

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_D = V_{DB} = 15V$ $V_{IN} = 5V, I_C = 75A,$ $T_J = 25^\circ C$	-	1.55	2.05	V
		$T_J = 125^\circ C$	-	1.65	2.10	
FWDi forward voltage	V_{EC}	$V_{IN} = 0V, -I_C = 75A$	-	1.70	2.20	V
Switching time	t_{on}	$V_{CC} = 300V, V_D = V_{DB} = 15V$ $I_C = 75A, V_{IN} = 0-5V$ $T_J = 125^\circ C$ Inductive load (upper-lower arm)	1.80	2.40	3.60	μs
	t_{rr}		-	0.30	-	
	$t_{c(on)}$		-	0.40	0.60	
	t_{off}		-	3.40	4.80	
	$t_{c(off)}$		-	0.60	1.20	
Collector-emitter cut-off current	I_{CES}	$V_{CE} = V_{CES}$ $T_J = 25^\circ C$	-	-	1	mA
		$T_J = 125^\circ C$	-	-	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

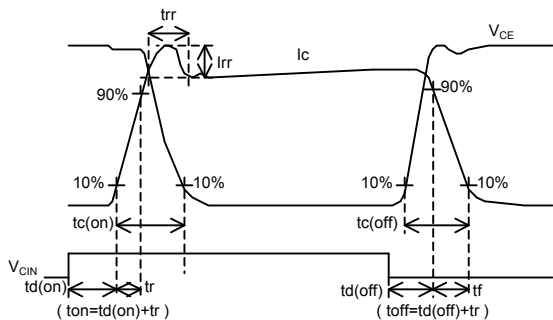


Fig.2-2 Switching time definition

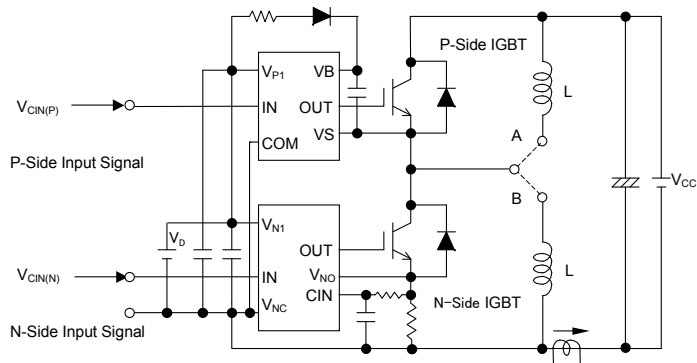


Fig.2-3 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation

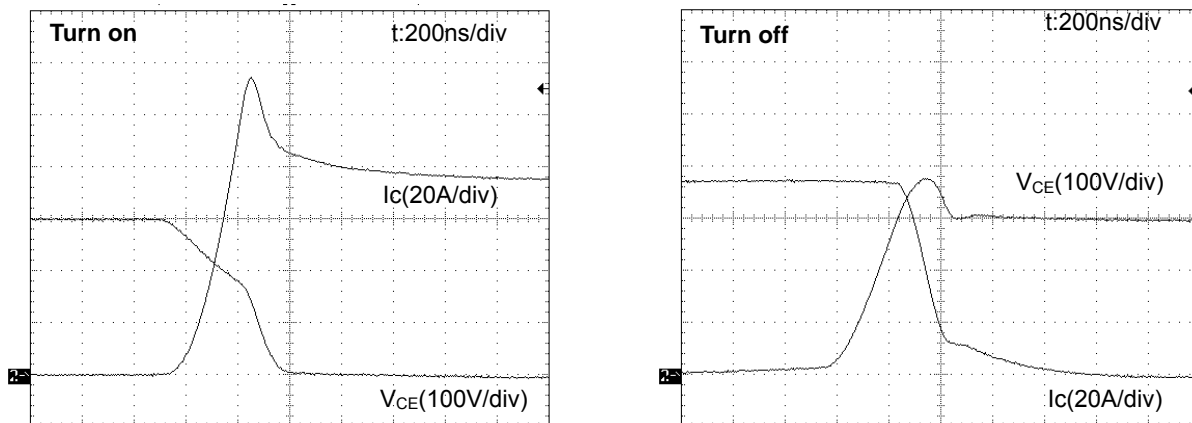


Fig.2-4 Typical switching waveform (PS21A7A)

Conditions : $V_{CC}=300V$, $V_D=V_{DB}=15V$, $T_j=125^\circ C$, $I_c=75A$, Inductive load half-bridge circuit

2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PS21A7A

Control (Protection) Part :

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I _D	V _D =V _{DB} =15V	Total of V _{P1} -V _{PC} ,V _{N1} -V _{NC}	-	-	5.50	mA
		V _{IN} =5V	V _{UFB} -V _{UFS} ,V _{VFB} -V _{VFS} ,V _{WFB} -V _{WFS}	-	-	0.55	
		V _D =V _{DB} =15V	Total of V _{P1} -V _{PC} ,V _{N1} -V _{NC}	-	-	5.50	
		V _{IN} =0V	V _{UFB} -V _{UFS} ,V _{VFB} -V _{VFS} ,V _{WFB} -V _{WFS}	-	-	0.55	
Fo output voltage	V _{FOH}	V _{SC} =0V, Fo terminal pull-up to 5V by 10kΩ		4.9	-	-	V
	V _{FOL}	V _{SC} =1V, I _{FO} =1mA		-	-	0.95	
Input current	I _{IN}	V _{IN} =5V		0.7	1.0	1.5	mA
Short circuit trip level (Note 3)	I _{SC}	-20°C≤T _C ≤100°C, R _S =23.2Ω (±1%), Not connecting outer shunt resistors to NU,NV,NW terminals		127	-	-	A
Control supply under- voltage protection	UV _{DBt}	T _C ≤100°C	Trip level	10.0	-	12.0	V
	UV _{DBr}		Reset level	10.5	-	12.5	
	UV _{Dt}		Trip level	10.3	-	12.5	
	UV _{Dr}		Reset level	10.8	-	13.0	
Fault output pulse width	t _{FO}	C _{FO} =22nF (Note 4)		1.6	2.4	-	ms
ON threshold voltage	V _{th(on)}	Applied between U _P ,V _P ,W _P -V _{PC} , U _N ,V _N ,W _N -V _{NC}		2.1	2.3	2.6	V
OFF threshold voltage	V _{th(off)}			0.8	1.4	2.1	
Temperature output	V _{OT}	At LVIC temperature=85°C (Note 5)		3.57	3.63	3.69	V

(Note 3) Short circuit (SC) protection is functioning only for N-side IGBTs.

(Note 4) Fault signal is output when the lower arms short circuit or control supply under-voltage protective functions operate.

The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} . ($t_{FO}(typ) = C_{FO} / (9.1 \times 10^6)$ [s])

(Note 5) DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively.

When temperature exceeds the protect level that customer defined, controller (MCU) should stop the DIPIPM.

2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS21A7A are given in Table 2-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIIPM safe operation.

Table 2-5 Recommended operating conditions of PS21A7A

Recommended Operation Conditions :

Item	Symbol	Condition		Recommended			Unit
				Min.	Typ.	Max.	
Supply voltage	V_{CC}	Applied between P-NU,NV,NW		0	300	400	V
Control supply voltage	V_D	Applied between $V_{P1}-V_{PC}$, $V_{N1}-V_{NC}$		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between $V_{UEB}-V_{UES}$, $V_{VEB}-V_{VES}$, $V_{WFB}-V_{WFS}$		13.0	15.0	18.5	V
Control supply variation	$\Delta V_D, \Delta V_{DB}$			-1	-	+1	V/ μ s
Arm-shoot-through blocking time	t_{dead}	For each input signal, $T_C \leq 100^{\circ}\text{C}$		2.7	-	-	μ s
PWM input frequency	f_{PWM}	$T_C \leq 100^{\circ}\text{C}$, $T_j \leq 125^{\circ}\text{C}$		-	-	20	kHz
Output rms current	I_O	$V_{CC}=300\text{V}$, $V_D=15\text{V}$ P.F=0.8 Sinusoidal PWM, $T_C \leq 100^{\circ}\text{C}$, $T_j \leq 125^{\circ}\text{C}$ (Note 7)	$f_{PWM}=5\text{kHz}$	-	-	35.0	A_{rms}
			$f_{PWM}=15\text{kHz}$	-	-	17.0	
Minimum input pulse width	PWIN(on)	(Note 8)		1.3	-	-	μ s
	PWIN(off)	$200 \leq V_{CC} \leq 350\text{V}$, $13.5 \leq V_D \leq 16.5\text{V}$, $13.5 \leq V_{DB} \leq 18.5\text{V}$, $-20 \leq T_C \leq 100^{\circ}\text{C}$, N line wiring inductance less than 10nH (Note 9)	$I_C \leq 75\text{A}$	3.0	-	-	
			$75 < I_C \leq 127.5\text{A}$	5.0	-	-	
V_{NC} variation	V_{NC}	Potential difference between $V_{NC}-\text{NU,NV,NW}$ including surge voltage		-5.0	-	+5.0	V
Junction temperature	T_j			-20	-	+125	$^{\circ}\text{C}$

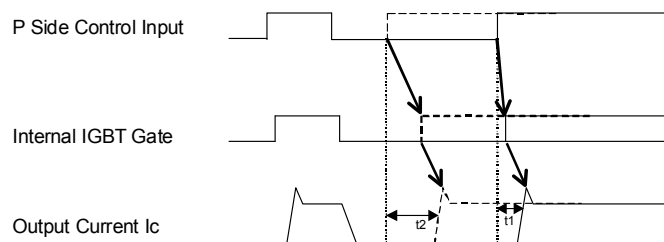
(Note 7) The allowable output rms current also depends on user application conditions.

(Note 8) Input signal with ON pulse width less than PWIN(on) might make no response.

(Note 9) IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).

Please refer below about delayed response .

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Real line: off pulse width > PWIN(off); turn on time t1

Broken line: off pulse width < PWIN(off); turn on time t2

2.1.6 Mechanical Characteristics and Ratings

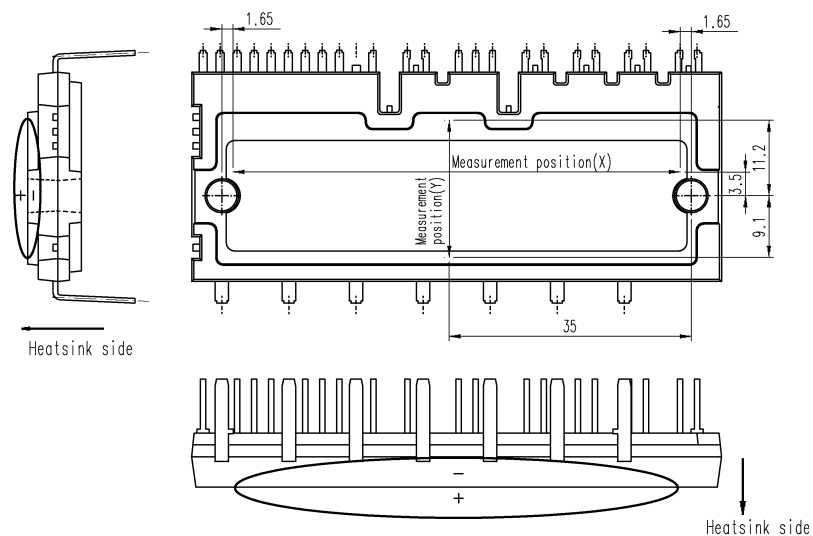
The mechanical characteristics and ratings are shown in Table 2-6
Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6 Mechanical characteristics and ratings of PS21A7A

Mechanical Characteristics and Ratings:

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: (M4)	Recommended: 1.18N·m	0.98	—	1.47	N·m
Weight			—	46	—	g
Heat sink side flatness	(Note 6)		−50	—	100	μm

Note 6: Flatness measurement position



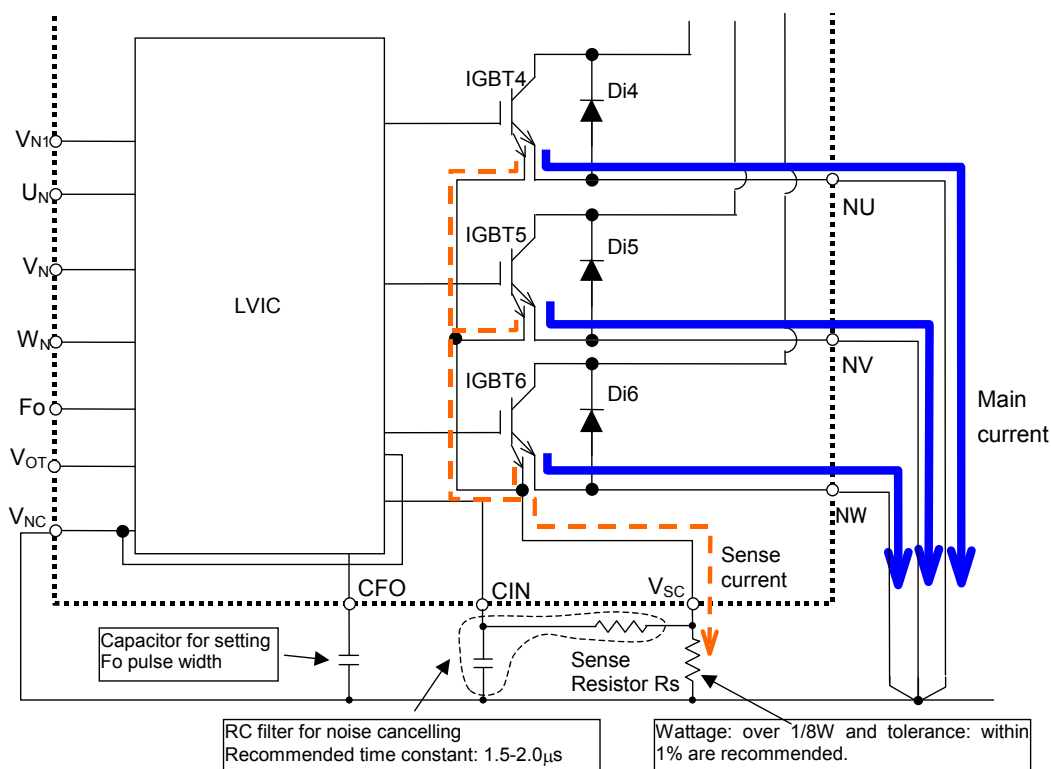
2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in the large DIIPM Ver.4. The detailed information are described below.

2.2.1 Short Circuit Protection

In large DIIPM Ver.4 series, the method of SC protection is different from current products, which detect main current by shunt resistor inserted into main current path.

But this SC protection detects much smaller sense current (split at N-side IGBT) by measuring the potential of sense resistor R_s , which is connected to V_{sc} terminal. So high wattage type shunt resistor isn't necessary for SC protection, and the loss at shunt resistor can be reduced. (Fig.2-5)



*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

Fig.2-5 SC protection circuit

SC protection works by feedback the potential, which is generated by sense current flowing into the sense resistor, to C_{IN} terminal. And when SC protection occurs, DIIPM shutdowns all N-side IGBTs hardly and outputs F_o signal. (its pulse width is set by C_{FO} capacitor.)

To prevent malfunction, it is recommended to insert RC filter before inputting to C_{IN} terminal and set the time constant to $1.5\mu\text{s}$ - $2.0\mu\text{s}$ because guaranteed short circuit protection capability of DIIPM is within $2\mu\text{s}$.

Table 2-7 SC protection trip level

	R_s	Min.	Typ.	Max.
PS21A7A	23.2Ω	127A	-	-
PS21A79	40.2Ω	85A	-	-

Condition: $T_j = -20^\circ\text{C} \sim 125^\circ\text{C}$, Not connecting outer shunt resistors to NU, NV, NW terminals

Normally, 23.2Ω and 40.2Ω (both E96 series) are recommended to PS21A7A and PS21A79 respectively.

If it is necessary to change the trip level, it can be achieved by changing sense resistance. But lower resistance than these values is not permitted.

The SC protection level depends on the sense resistance and the temperature. Their characteristics vs. sense resistance for PS21A7A and PS21A79 are described as Fig.2-6 and Fig.2-7.

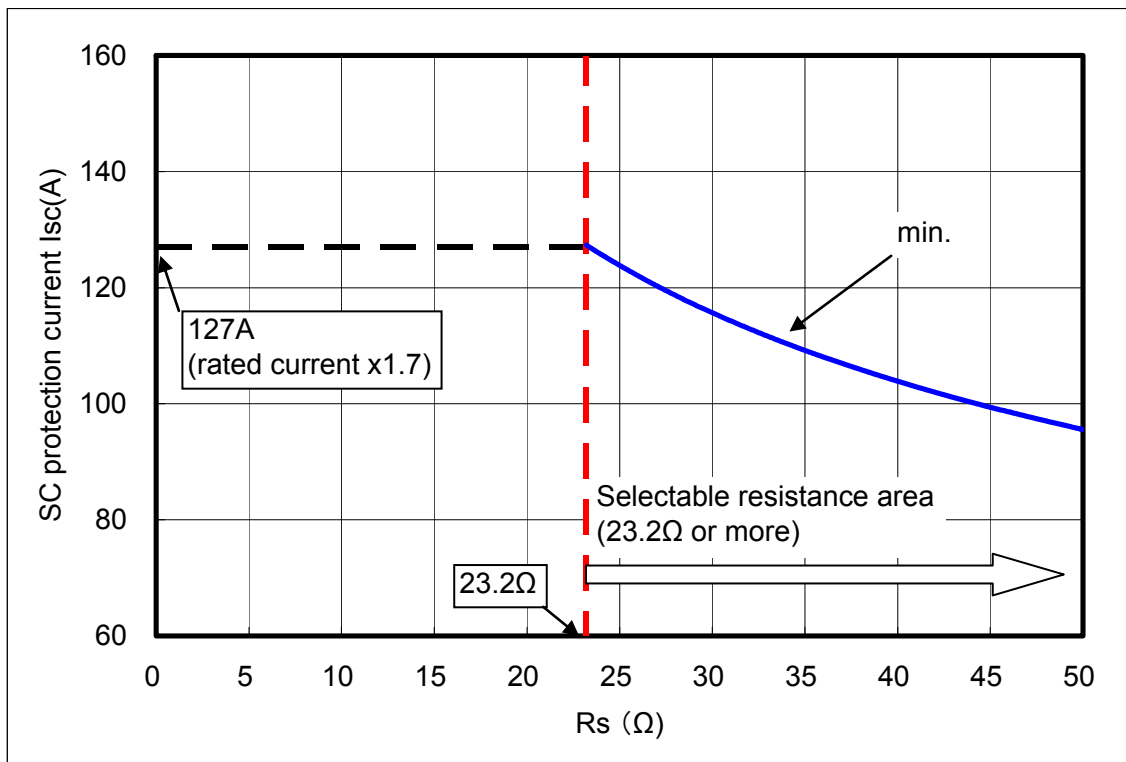


Fig.2-6 Sense resistance R_s vs. SC trip level for PS21A7A
($T_j = -20 \sim 125^\circ\text{C}$, Not connecting outer shunt resistors to NU, NV, NW terminals)

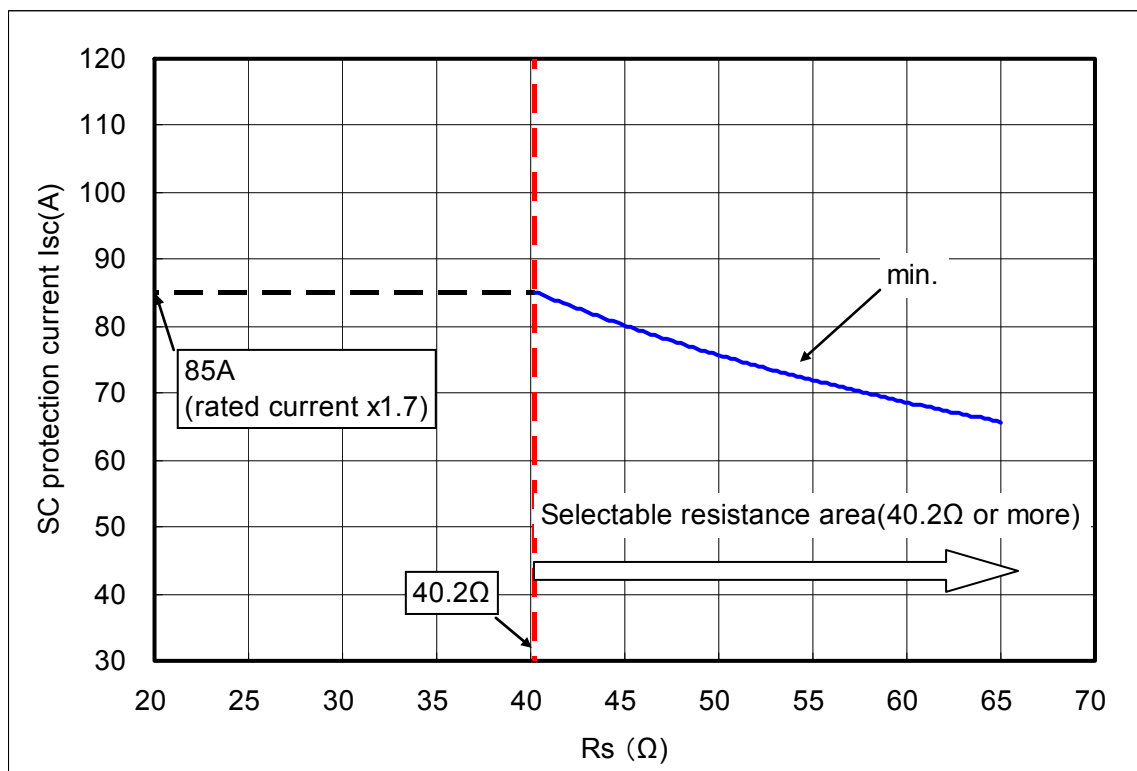


Fig.2-7 Sense resistance R_s vs. SC trip level for PS21A79
($T_j = -20 \sim 125^\circ\text{C}$, Not connecting outer shunt resistors to NU, NV, NW terminals)

For sense resistor, its big fluctuation leads to big fluctuation of SC trip level. So it is necessary to select small variation in the resistance (within $\pm 1\%$ is recommended).

And its wattage can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 3000:1 for PS21A7A and PS21A79. (In this case maximum sense current flows.) The estimation example for PS21A7A is described as below.

[Estimation example]

(1) Normal operation state

It is assumed that the maximum main current for normal operation is 150A (rated current x 2, for keeping a margin) and the sense resistance is 23.2Ω.

In this case, The maximum sense current flows through the sense resistor is calculated as below.

$$150\text{A} / 3000 = 50\text{mA}$$

And the loss at the sense resistor is

$$P = I^2 \cdot R \cdot t = (50\text{mA})^2 \times 23.2\Omega \times 1\text{s} = \underline{58\text{mW}}$$

(2) Short circuit state

When short circuit occurs, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =750A) flows. So the sense current is

$$750\text{A} / 3000 = 250\text{mA}$$

But this current shut down within 2μs by SC protection. And the loss at the sense resistor is

$$P = I^2 \cdot R \cdot t = (250\text{mA})^2 \times 23.2\Omega \times 2\mu\text{s} = \underline{0.0029\text{mW}}$$

As explained above, over 1/8W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]

It takes more time (like as Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC's transfer delay)

Table 2-8. Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and the this IC delay.

SC protection (N-side only, with external resistor and RC filter)

- a1. Normal operation: IGBT turn on and carry current.
- a2. Short circuit current is detected (SC trigger).
- a3. All N-side IGBTs' gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo output with a fixed pulse width (determined by the external capacitance C_{FO}).
- a6. Input "L": IGBT off.
- a7. Input "H": IGBT on, but during the Fo output period the IGBT will not turn on.
- a8. IGBT turns ON when L→H signal is input after Fo is reset.

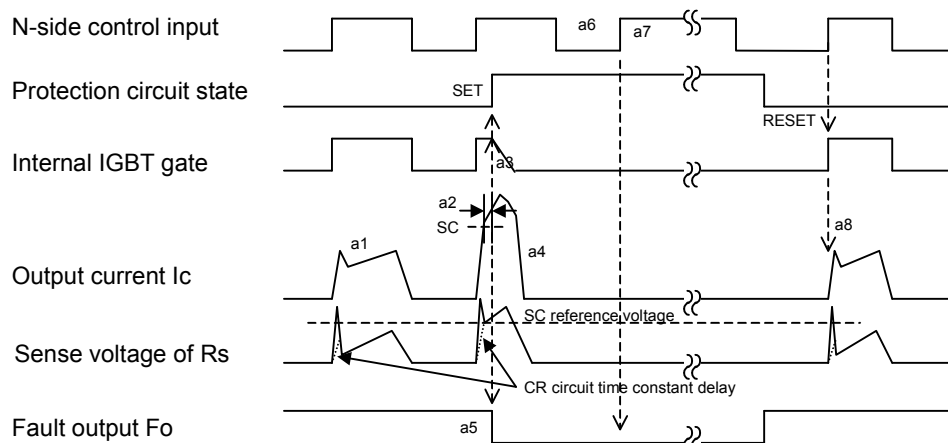


Fig.2-8 SC protection timing chart

2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-9.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-9 DIIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-signals to DIIPM before the control supply coming up to 13.5V)
4.0-UV trip level (P, N)	UV function become active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV trip level-13.5V(N),13.0V(P)	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions. (Normal operation)
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	Over maximum voltage rating. The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq \pm 1V/\mu s, \quad V_{\text{ripple}} \leq 2V_{\text{p-p}}$$

N-side UV Protection Sequence

- a1. Control supply voltage V_D rises: After V_D level reaches under voltage reset level (UV_{Dr}), the circuits start to operate when next input is applied.
- a2. Normal operation: IGBT turn on and carry current.
- a3. V_D level dips to under voltage trip level. (UV_{Dt}).
- a4. All N-side IGBTs turn OFF in spite of control input condition.
- a5. Fo is output for the period determined by the capacitance C_{FO} but continuously during UV period.
- a6. V_D level reaches UV_{Dr} .
- a7. Normal operation: IGBT turn on and carry current.

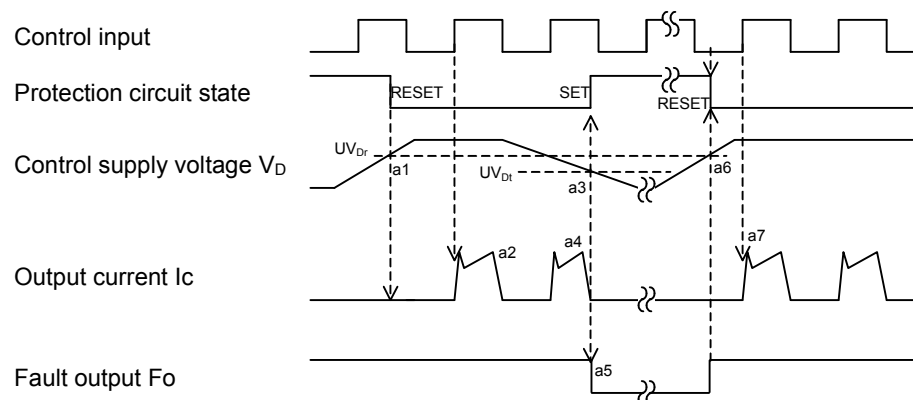


Fig.2-9 Timing chart of N-side UV protection

P-side UV Protection Sequence

- b1. Control supply voltage V_{DB} rises : After V_{DB} level reaches under voltage reset level (UV_{DBr}), the circuits start to operate when next input is applied.
- b2. Normal operation: IGBT turn on and carry current.
- b3. V_{DB} level dips to under voltage trip level (UV_{DBt}).
- b4. P-side IGBT turns OFF in spite of control input signal level, but there is no Fo signal output.
- b5. V_{DB} level reaches UV_{DBr} .
- b6. Normal operation: IGBT turn on and carry current.

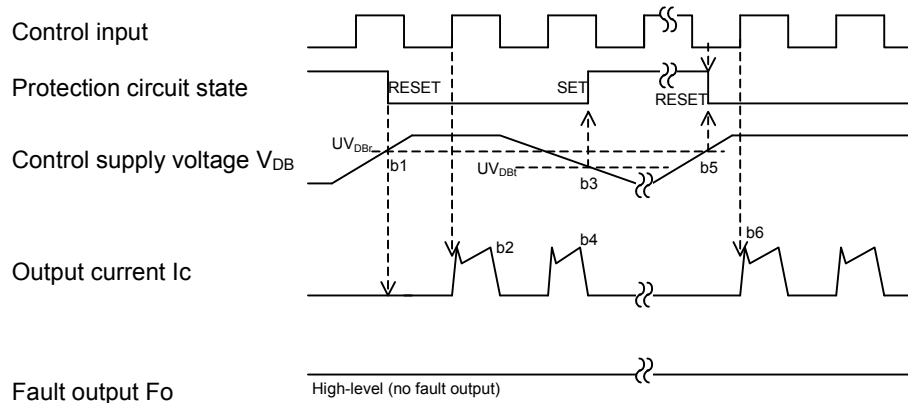


Fig.2-10 Timing Chart of P-side UV protection

2.2.3 Temperature analog output

(1) Purpose of this function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)

It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was set on outer heat sink currently)

[Note]

DIPIM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIPIM.

(2) V_{OT} characteristics

The characteristics of V_{OT} output vs. LVIC temperature is described as Fig.2-11.

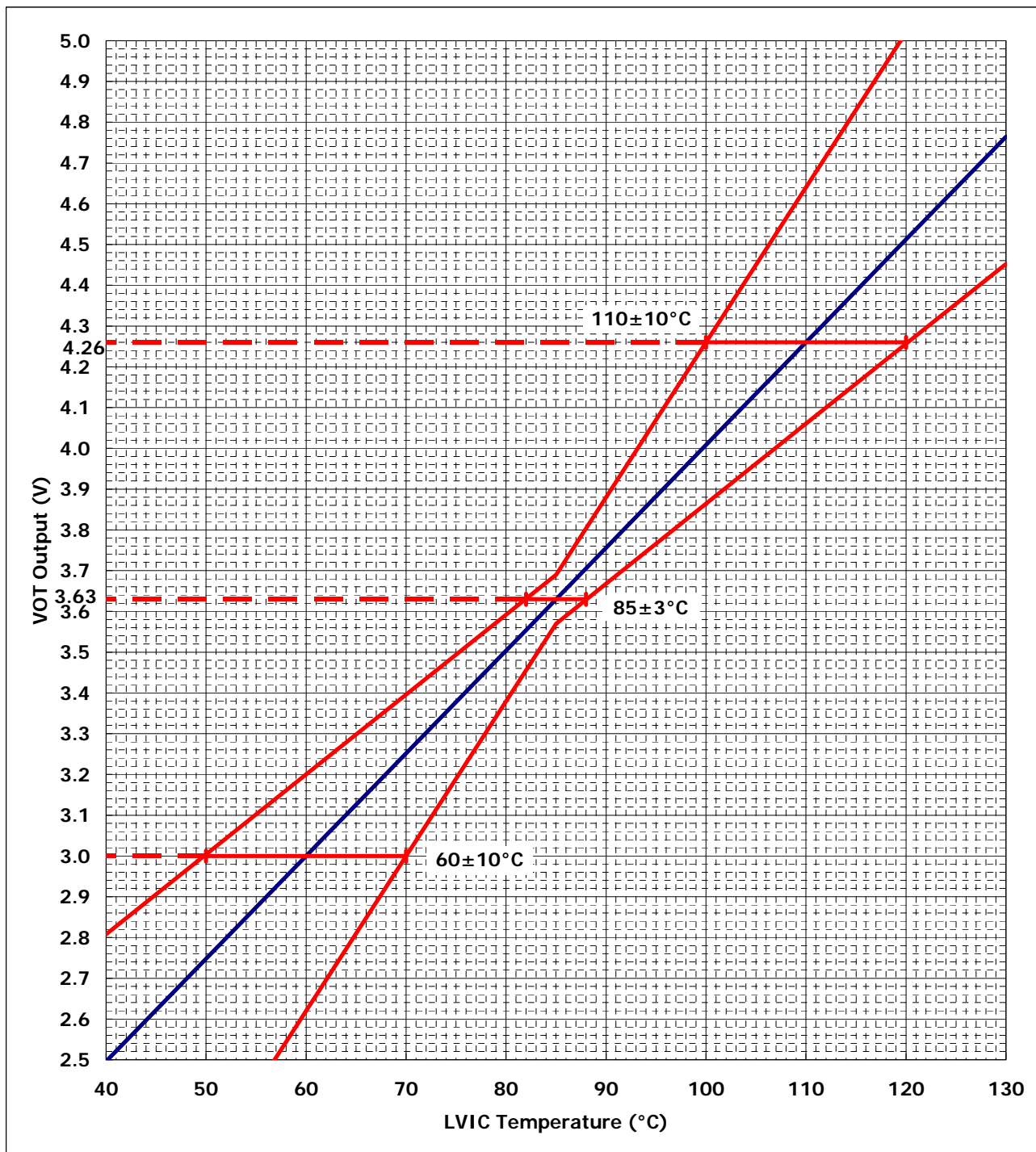


Fig.2-11 V_{OT} output vs. LVIC temperature

As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature: $T_{ic}(=V_{OT} \text{ output})$, case temperature: T_c (measuring point is defined on datasheet), and junction temperature: T_j depends on the system cooling condition, heat sink, control strategy, etc.

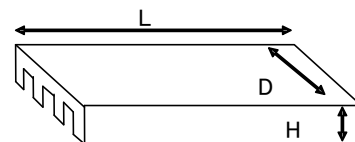
For example, the evaluation results in the case of using different size heat sink (table 2-10) are described as Fig.2-12. As the result of evaluations, it is clear that two cases have different relationships between LVIC temperature T_{ic} and case temperature T_c .

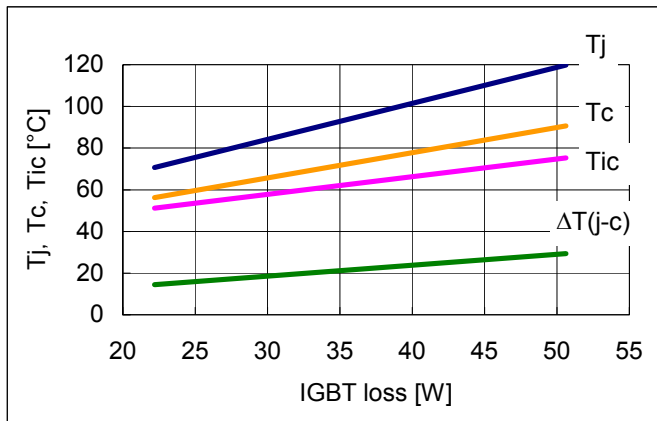
So when setting the threshold temperature for protection, it is necessary to measure the relationship between them on your real system. And when setting threshold temperature T_{ic} , it is important to consider the protection temperature is at $T_c \leq 100^\circ\text{C}$ and $T_j \leq 150^\circ\text{C}$.

Measuring each temperatures @ only 1 IGBT chip turns on (DC current, $T_a=25^\circ\text{C}$)

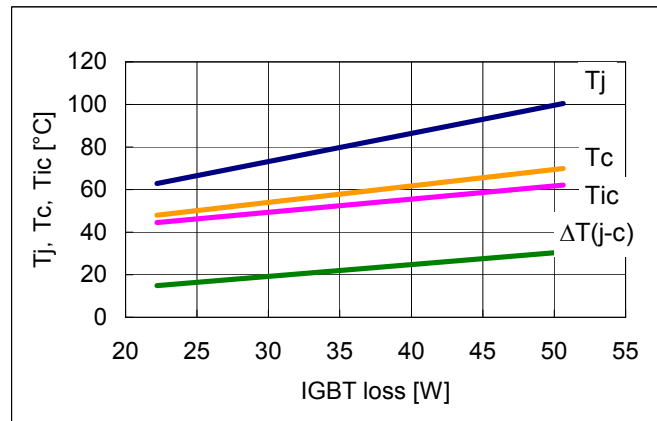
Table 2-10 Outer heat sink

	Thermal resistance $R_{th}(f-a)$	Heat sink size ($L \times D \times H$)
A	2.20K/W	100 x 88 x 40 mm
B	1.35K/W	200 x 88 x 40 mm





(a) Heat sink A



(b) Heat sink B

Fig.2-12 IGBT loss vs. T_j , T_c , T_{ic} ($T_a=25^\circ\text{C}$, Typical)

The procedure example of setting protection temperature is described below.

Fig.2-13 indicates the example of the relationship between LVIC temperature T_{ic} , case temperature T_c and junction temperature T_j , and Fig.2-14 is the relationship between V_{OT} and T_c , which is obtained by combining Fig.2-11 and Fig.2-13.

If the protection level is set to $T_j=125^\circ\text{C}$ ($T_c=100^\circ\text{C}$), then V_{OT} threshold level should be set 3.75V which is the maximum value @ $T_c=100^\circ\text{C}$ in Fig.2-14.

In this case the variation of real T_c may become from 100°C to 115°C . But even if the real T_c will be maximum variation value 115°C , T_j becomes under 150°C ($125^\circ\text{C}+15^\circ\text{C}=140^\circ\text{C}<150^\circ\text{C}$).

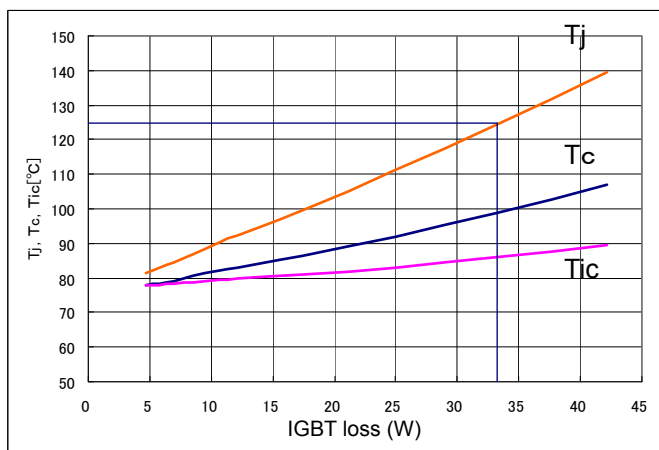


Fig.2-13 IGBT loss vs. T_j , T_c , T_{ic} (Typical) ($T_a=80^\circ\text{C}$)

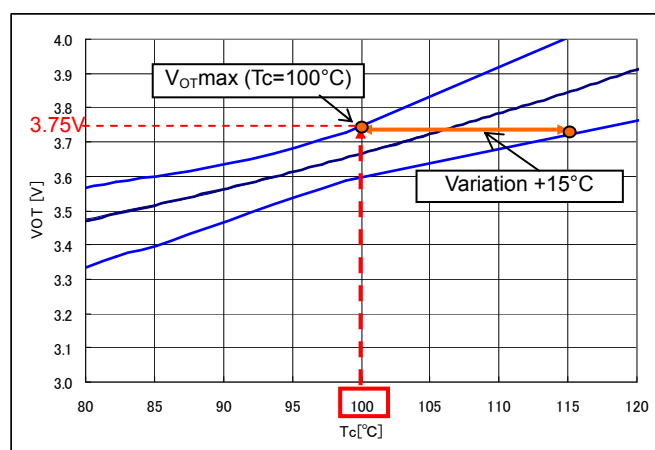


Fig.2-14 V_{OT} vs. T_c (Typical)

As mentioned above, the relationship between T_{ic} , T_c and T_j depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V_{OT} vs. LVIC temperature and the thermocouple for measuring T_j .

(3) Inner circuit of V_{OT} terminal

Inner circuit of V_{OT} terminal is the output of OP amplifier circuit and is described as Fig.2-15

If the resistor is inserted between V_{OT} and V_{NC} (control supply GND) terminals, then the current (calculated by V_{OT} output \div resistance of inserted resistor) always flows as circuit current of LVIC.

The current capability of V_{OT} output is described as Table 2-11.

Table 2-11 Output capability ($T_c=-20^\circ\text{C}\sim 100^\circ\text{C}$)

	min.
Source	1.7mA
Sink	0.1mA

Source : the current flow from V_{OT} to outside.

Sink : the current flow from outside to V_{OT} .

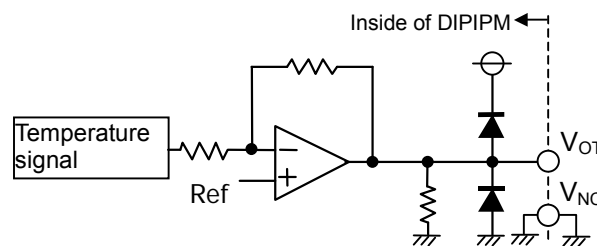


Fig.2-15 Inner circuit of V_{OT} terminal

2.3 Package Outlines

2.3.1 Outline Drawing

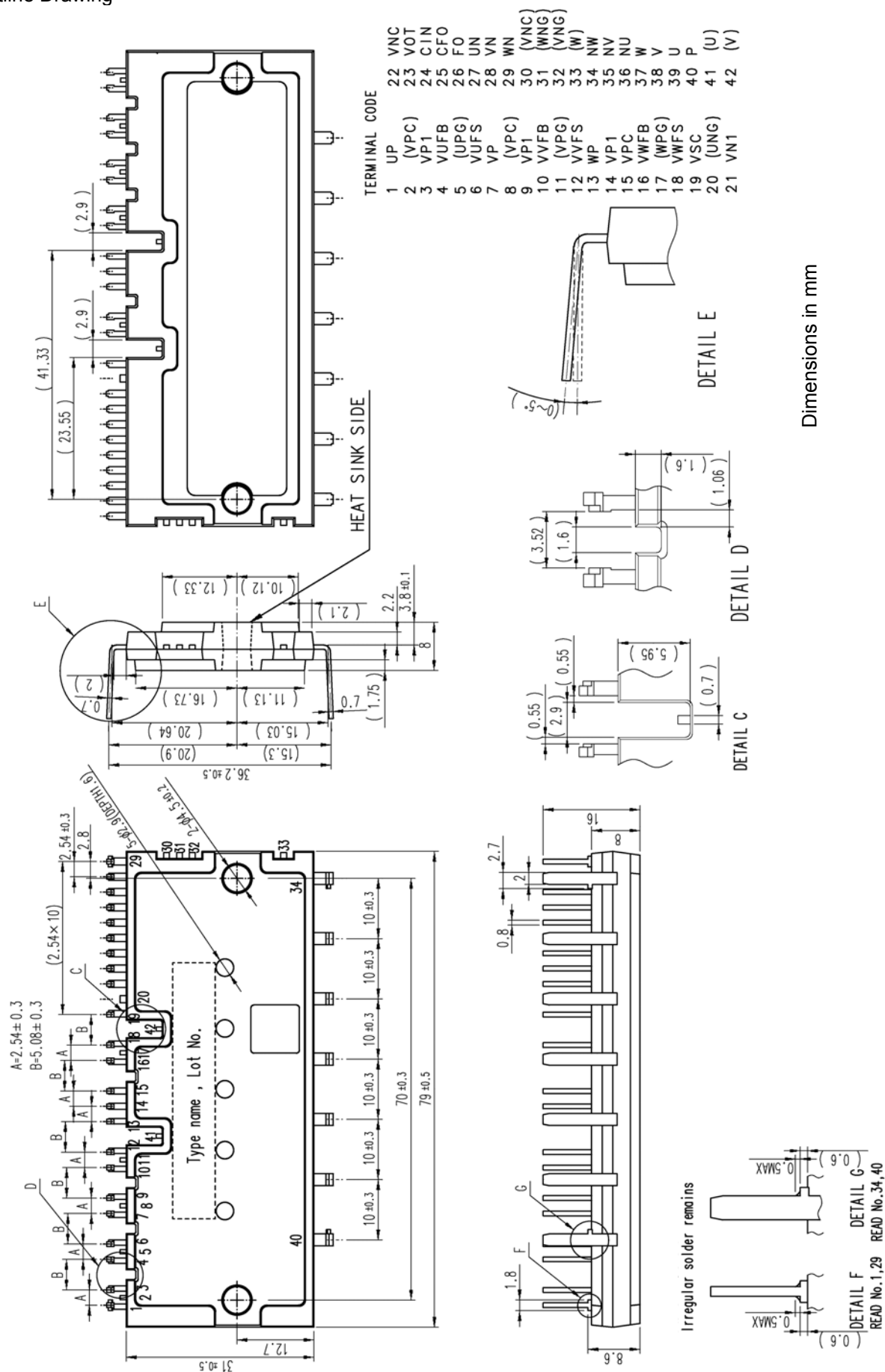


Fig.2-16 Outline drawing

2.3.2 Power Chip Position

Fig.2-17 indicates the center position of the each power chips.
(This figure is the view from laser marked side.)

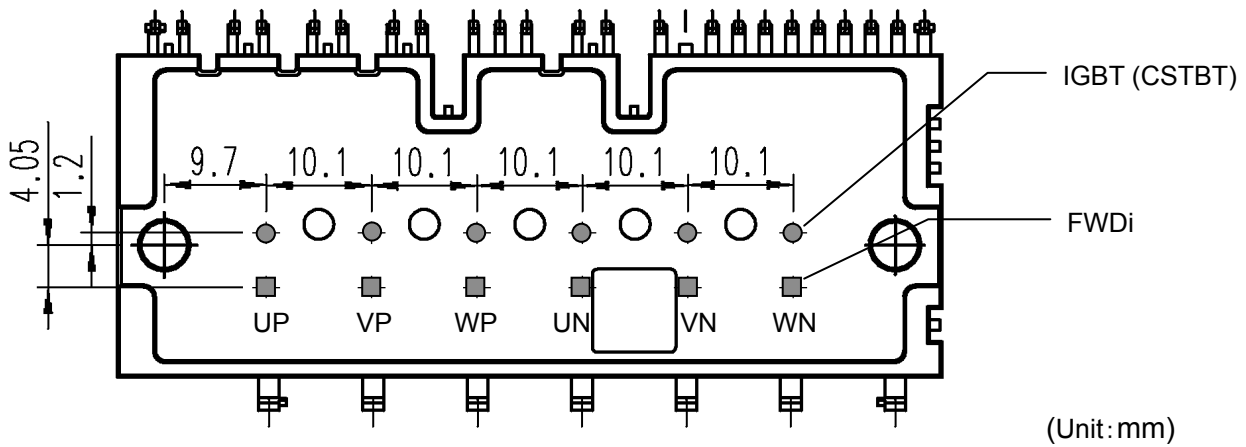
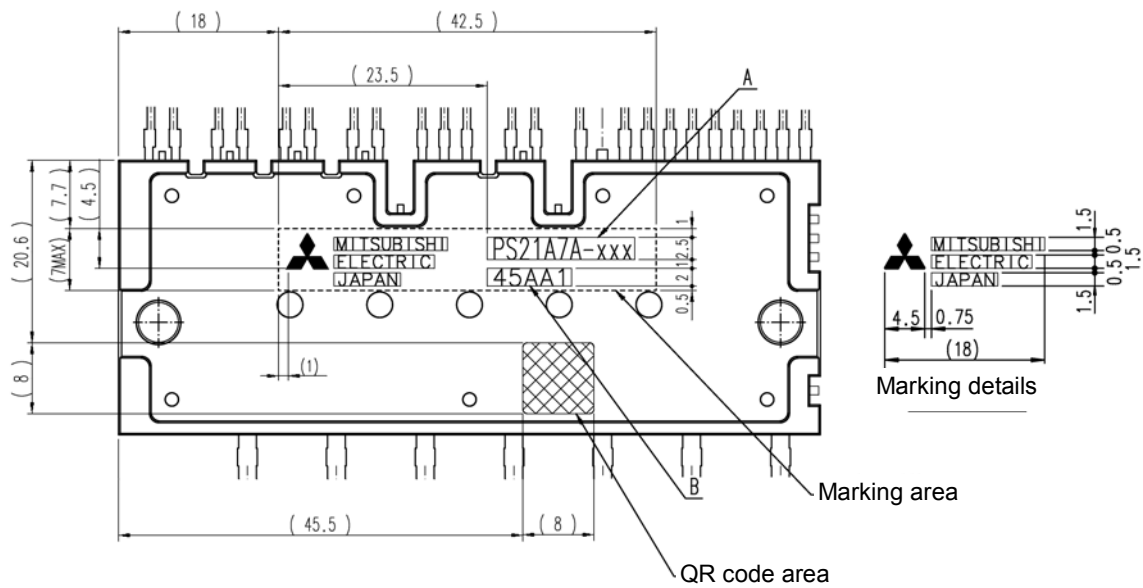


Fig.2-17 Power chip position

2.3.3 Laser Marking Position

The laser marking specification is described in Fig.2-18.
Mitsubishi Corporation mark, Type name (A), Lot number (B), and QR code mark are marked in the upper side of module.



QR Code is registered trademark of DENSO WAVE INCORPORATED in JAPAN and other countries.
Fig.2-18 Laser marking view

2.3.4 Terminal Description

Table 2-12 Terminal description

No.	Name	Description
1	U _P	U-phase P-side control input terminal
3	V _{P1}	U-phase P-side control supply positive terminal
4	V _{UFB}	U-phase P-side drive supply positive terminal
6	V _{UFS}	U-phase P-side drive supply GND terminal
7	V _P	V-phase P-side control input terminal
9	V _{P1}	V-phase P-side control supply positive terminal
10	V _{VFB}	V-phase P-side drive supply positive terminal
12	V _{VFS}	V-phase P-side drive supply GND terminal
13	W _P	W-phase P-side control input terminal
14	V _{P1}	W-phase P-side control supply positive terminal
15	V _{PC}	P-side control supply GND terminal
16	V _{WFB}	W-phase P-side drive supply positive terminal
18	V _{WFS}	W-phase P-side drive supply GND terminal
19	V _{SC}	Sense current detecting terminal
21	V _{N1}	N-side control supply positive terminal
22	V _{NC}	N-side control supply GND terminal
23	V _{OT}	LVIC temperature output terminal
24	CIN	SC trip voltage detect terminal
25	CFO	Fault pulse output width set terminal
26	F _O	Fault signal output terminal
27	U _N	U-phase N-side control input terminal
28	V _N	V-phase N-side control input terminal
29	W _N	W-phase N-side control input terminal
34	NW	W-phase N-side IGBT emitter terminal
35	NV	V-phase N-side IGBT emitter terminal
36	NU	U-phase N-side IGBT emitter terminal
37	W	W-phase output terminal
38	V	V-phase output terminal
39	U	U-phase output terminal
40	P	Inverter DC-link positive terminal

No.	Name	Description
2	V _{PC}	Internal use (Dummy pin) Don't connect all dummy pins to any other terminals or PCB pattern. (Leave no connect)
5	U _{PG}	
8	V _{PC}	
11	V _{PG}	
17	W _{PG}	
20	U _{NG}	
30	V _{NC}	
31	W _{NG}	
32	V _{NG}	
33	W	
41	U	
42	V	



Table 2-13 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal	V_{UFB} - V_{UFS} V_{VFB} - V_{VFS} V_{WFB} - V_{WFS}	<ul style="list-style-type: none"> • Drive supply terminals for P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIPIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side drive supply GND terminal		
P-side control supply terminal	V_{P1} V_{N1}	<ul style="list-style-type: none"> • Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control supply terminal		
N-side control GND terminal	V_{PC} V_{NC}	<ul style="list-style-type: none"> • Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P, V_P, W_P U_N, V_N, W_N	<ul style="list-style-type: none"> • Control signal input terminals. • Voltage input type. These terminals are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Use RC coupling in case of signal oscillation. (Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Sense current detect terminal	V_{SC}	<ul style="list-style-type: none"> • The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.
Short-circuit trip voltage detecting terminal	CIN	<ul style="list-style-type: none"> • Input the potential of V_{SC} terminal (with sense resistor) to CIN terminal for SC protection through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	<ul style="list-style-type: none"> • Fault signal output terminal for N-side abnormal state(SC or UV). • This output is open drain type. F_O signal line should be pulled up to a 5V logic supply with over 5kΩ resistor (for limiting the F_O sink current I_{FO} up to 1mA.) Normally 10kΩ is recommended.
Fault pulse output width setting terminal	CFO	<ul style="list-style-type: none"> • The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and VNC. • When 22nF capacitor is connected, then the F_O pulse width becomes 2.4ms. $t_{FO} = C_{FO} / (9.1 \times 10^{-6})$ (s)
Inverter DC-link positive terminal	P	<ul style="list-style-type: none"> • DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU, NV, NW	<ul style="list-style-type: none"> • Open emitter terminal of each N-side IGBT • If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible.
Inverter power output terminal	U, V, W	<ul style="list-style-type: none"> • Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1 μ s/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions.

2.4.1 Electric Spacing

The electric spacing specification of Large DIPIM Ver.4 is shown in Table 2-14

Table 2-14 Minimum insulation distance

	Clearance (mm)	Creepage (mm)
Between live power terminals with high potential	7.1	7.9
Between live control terminals with high potential	3.3	5.6
Between terminals and heat sink	3.7	5.6

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the device. The recommended fastening procedure is shown in Fig.2-19. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.

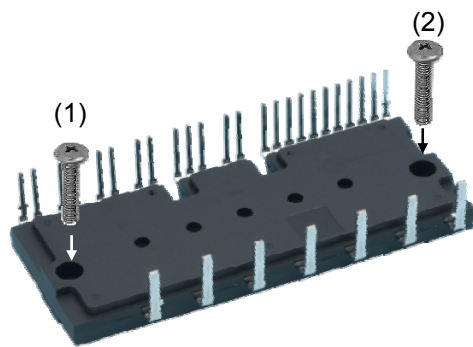


Fig.2-19 Recommended screw fastening order

Temporary fastening

(1)→(2)

Permanent fastening

(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Table 2-15. Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 1.18N·m, Screw : M4	0.98	-	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-20	-50	-	+100	μm

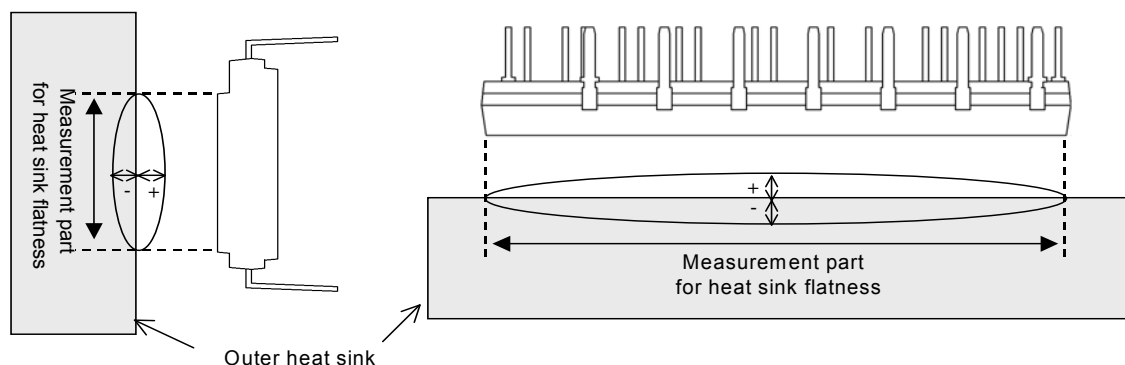


Fig.2-20 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIPIM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in table 2-16 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-16 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept under 150°C for considering glass transition temperature (T_g) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample : Large DIPIPM Ver.4

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe.
- (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

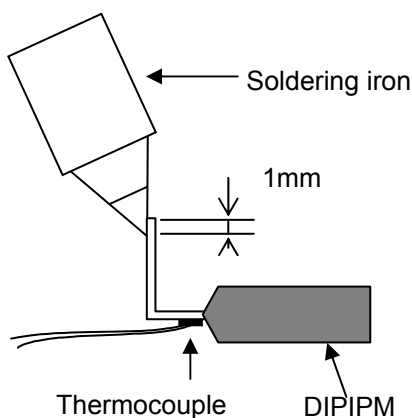


Fig.2-21 Heating and measuring point

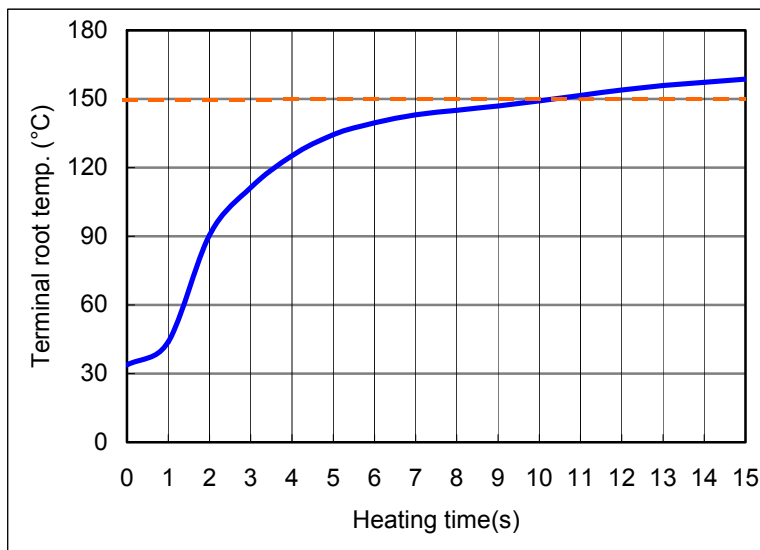


Fig.2-22 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance

This chapter states usage and interface circuit design hints.

3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics

Note: the capacitance also depends on the PWM control strategy of the application system

C2: 0.22 μ -2 μ F ceramic capacitor with good temperature, frequency and DC bias characteristics

C3: 0.1 μ -0.22 μ F Film capacitor (for snubber)

D1: Bootstrap diode. High speed type with V_{RRM} : over $V_{ces}(=600V)$, trr: up to 100ns

D2: Zener diode 24V/1W for surge absorber

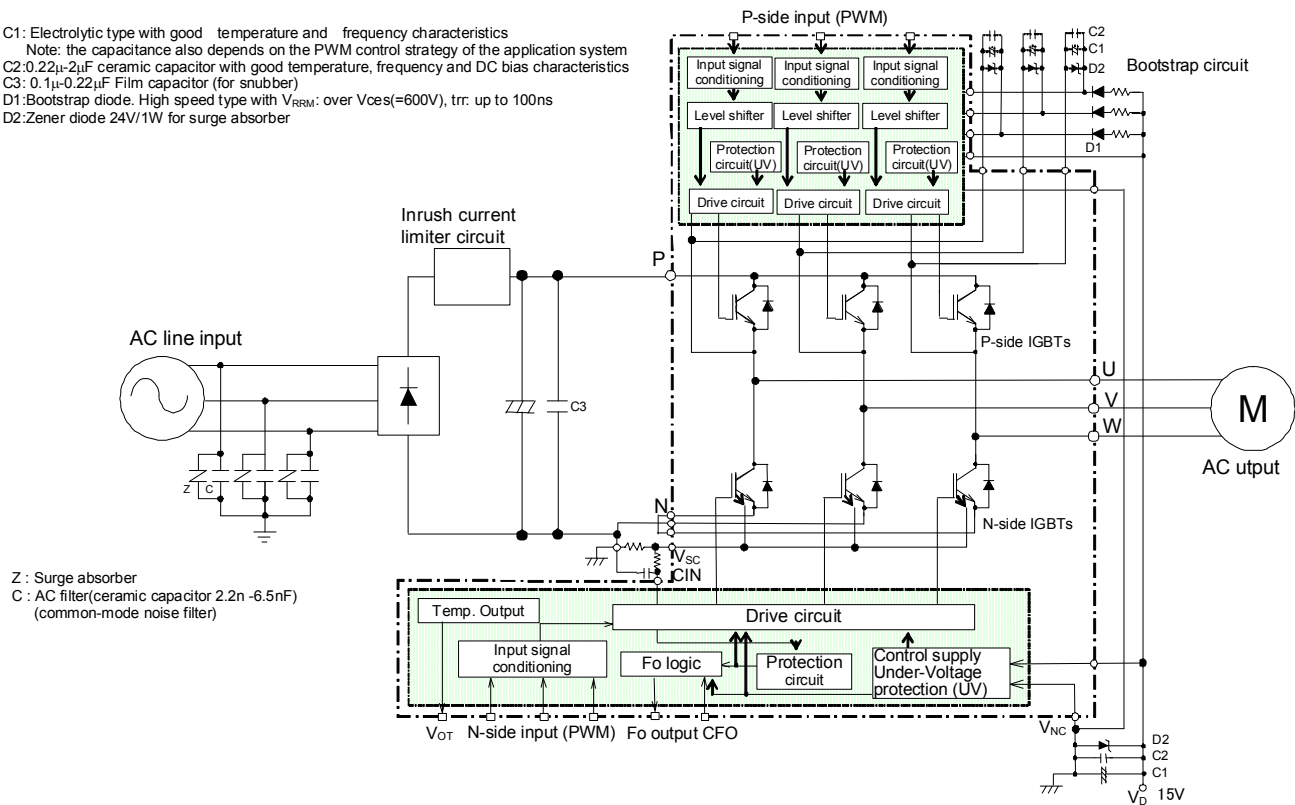


Fig.3-1 Application System block diagram



3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

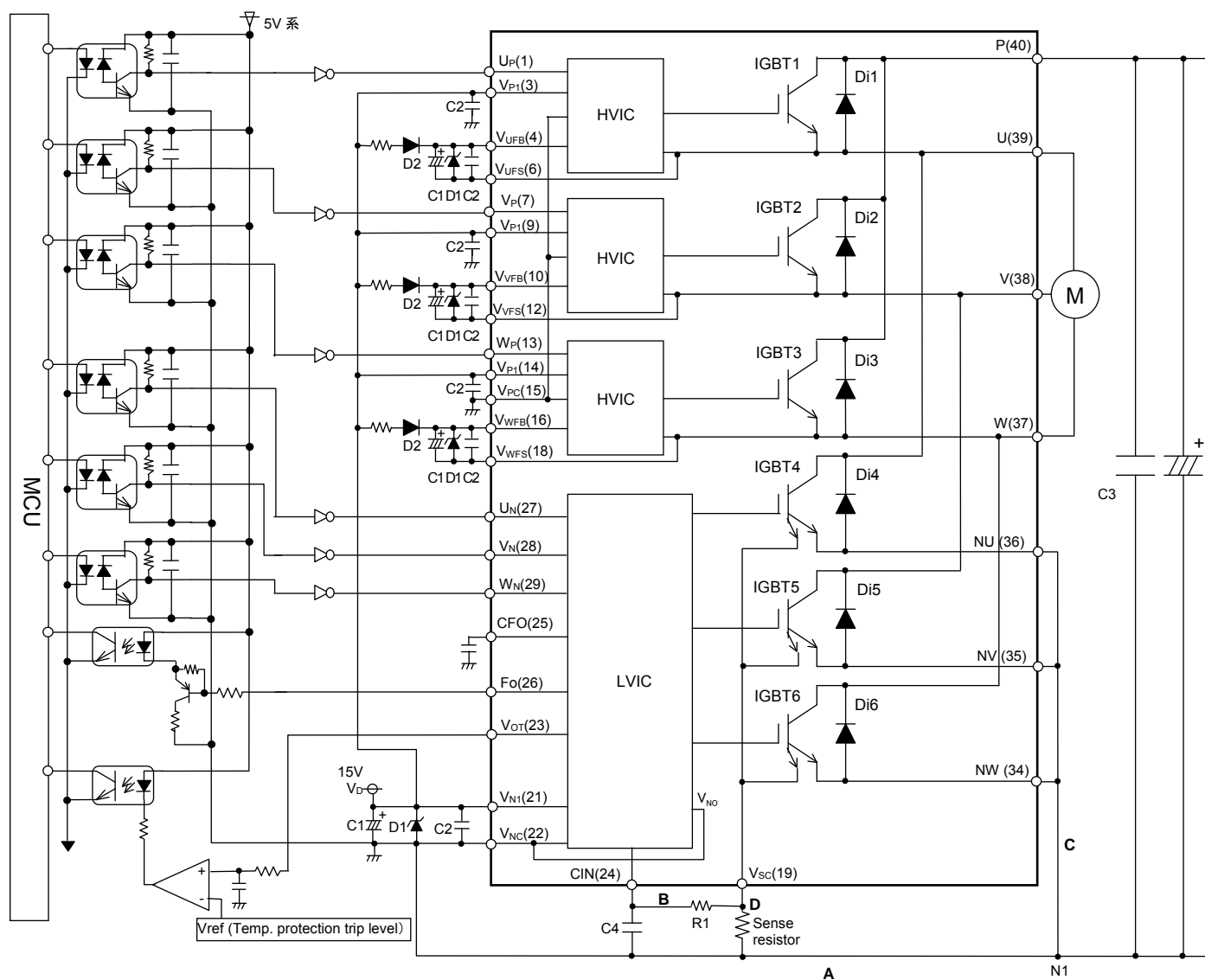


Fig.3-3 Interface circuit example with opto-coupler

Note:

- (1) High speed (high CMR) opto-coupler is recommended.
- (2) F_o terminal sink current is max. 1mA. A buffer circuit is necessary to drive an opto-coupler.

3.1.4 Circuits of Signal Input terminals and Fo Terminal

Large DIPIPM Ver.4 is high-active input logic. A 3.3k Ω (min) pull-down resistor is built-in each input circuit of the DIPIPM as shown in Fig.3-7, so external pull-down resistor is not needed.

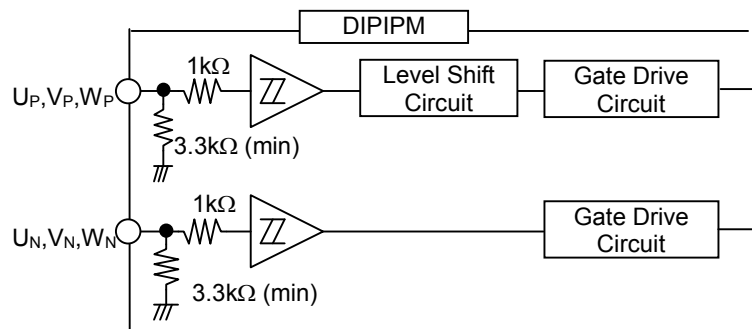


Fig.3-4 Internal structure of control input terminals

Table 3-1 Input threshold voltage ratings (T_j=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	V _{th(on)}	U _P , V _P , W _P -V _{PC}	2.1	2.3	2.6	V
Turn-off threshold voltage	V _{th(off)}	U _N , V _N , W _N -V _{NC}	0.8	1.4	2.1	

The wiring of each input should be patterned as short as possible. And if the pattern is long and the noise is imposed on the pattern, it may be effective to insert RC filter.

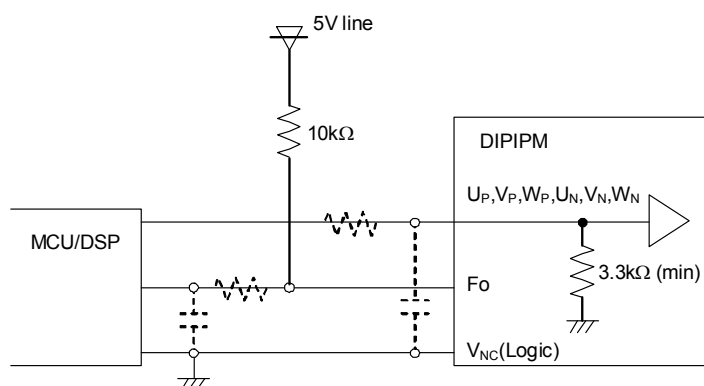


Fig.3-5 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.

The DIPIPM signal input section integrates a 3.3k Ω (min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

There are limits for the minimum input pulse width in the DIIPM. The DIIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Please refer Table 3-2)

Table 3-2 Allowable minimum input pulse width

	Symbol	Condition		PN	Min. value	Unit
On signal	PWIN(on)	-		PS21A79	1.1	μs
				PS21A7A	1.3	
Off signal	PWIN(off)	$200 \leq V_{CC} \leq 350\text{V}$, $13.5 \leq V_D \leq 16.5\text{V}$, $13.5 \leq V_{DB} \leq 18.5\text{V}$, $-20 \leq T_C \leq 100^\circ\text{C}$, N line wiring inductance less than 10nH	Up to rated current	PS21A79	3.0	
				PS21A7A	3.0	
			From rated current to 1.7x rated current	PS21A79	5.0	
				PS21A7A	5.0	

*) Input signal with ON pulse width less than PWIN(on) might make no response.
 IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).
 Please refer Fig.3-6 about delayed response .

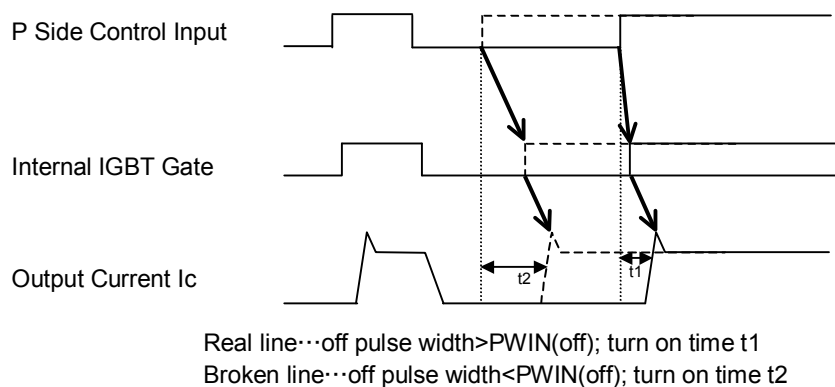


Fig.3-6 Delayed Response with shorter input off (P-side only)

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to control supply (e.g. 5V) as shown in Fig.3-5. Fig.3-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. (I_{F0} can be calculated from $I_{F0} = \text{control supply voltage} / \text{pull up resistance}$ approximately.) If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-3 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V _{FOH}	V _{SC} =0V, F _O =10kΩ, 5V pulled-up	4.9	-	-	V
	V _{FOL}	V _{SC} =1V, F _O =1mA	-	-	0.95	V

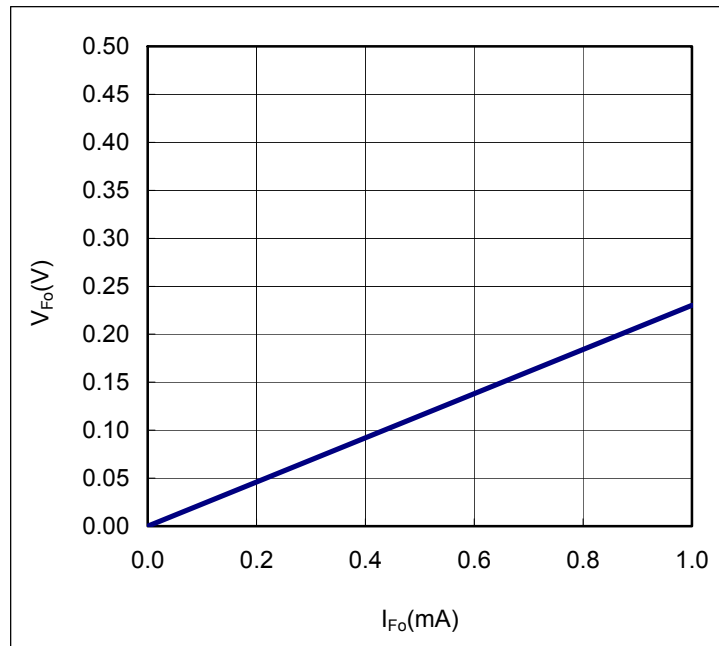


Fig.3-7 Fo terminal typical V-I characteristics (V_D=15V, T_J=25°C)

3.1.5 Snubber Circuit

In order to prevent DIPIPM from the surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.

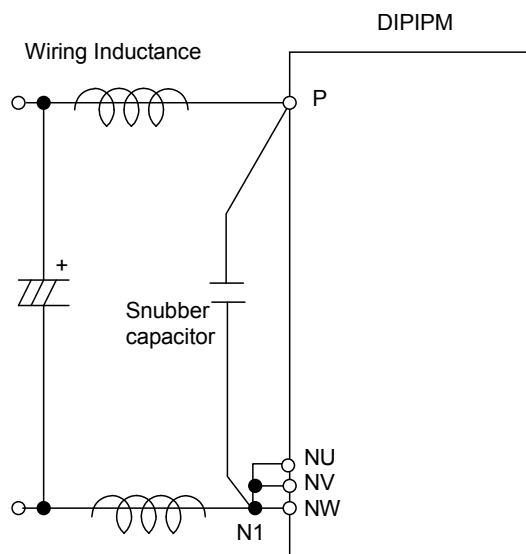


Fig.3-8 Recommended snubber circuit position

3.1.6 Influence of wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

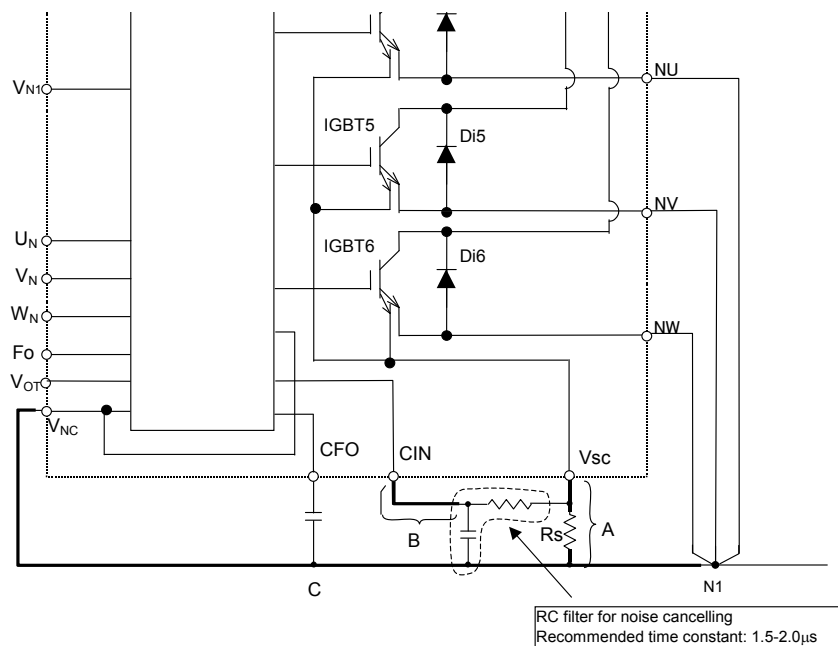


Fig.3-9 External protection circuit

(1) Influence of the part-A wiring

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) Influence of the part-B wiring pattern

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will drop down and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, VNC terminals as close as possible.

(3) Influence of the part-D wiring pattern

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

3.1.7 Precaution for wiring on PCB

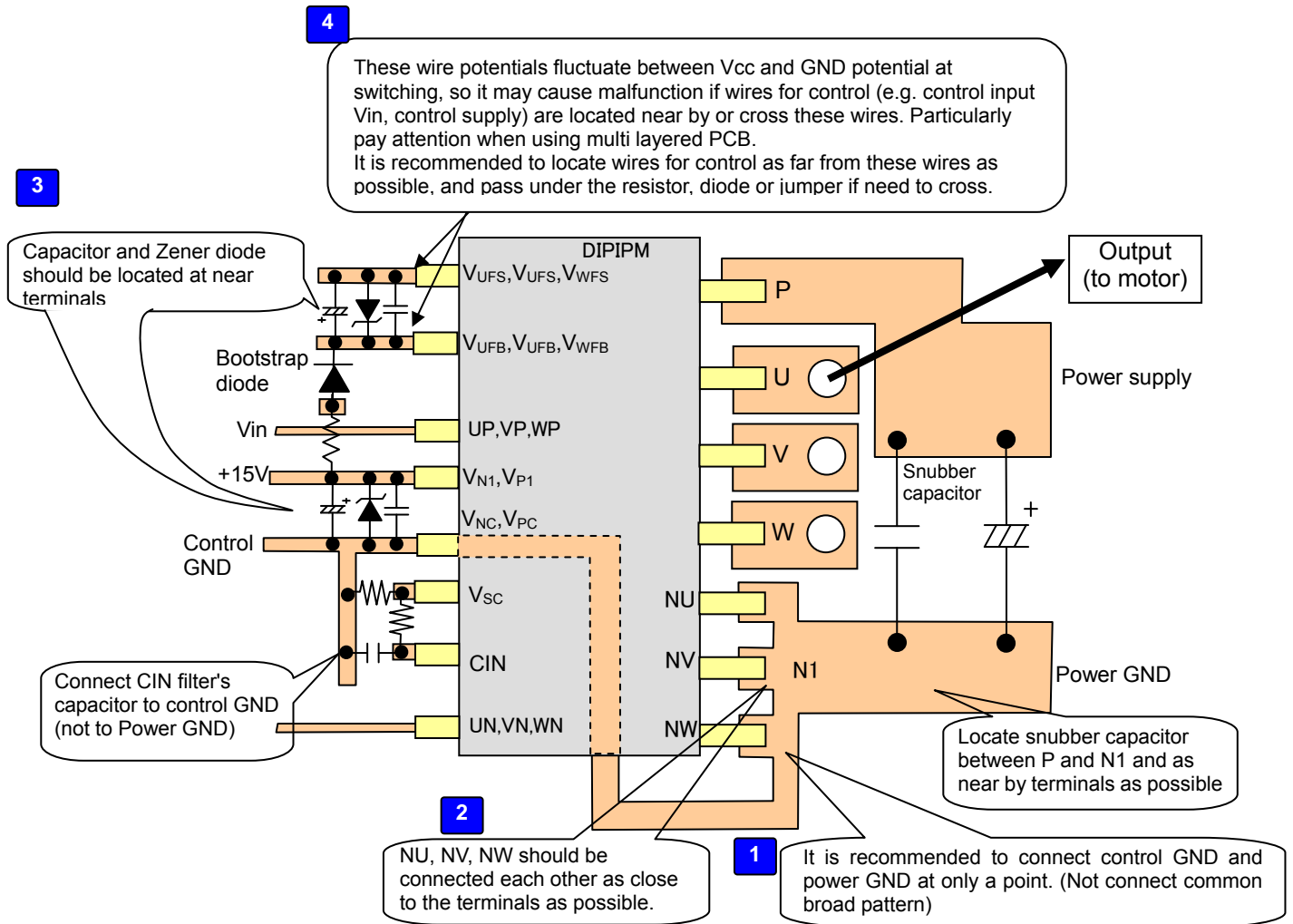


Fig.3-10 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	<ul style="list-style-type: none"> Control GND pattern overlaps power GND pattern. Ground loop pattern is existing. 	<p>The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. it causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.</p> <p>Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs.</p>
2	Long pattern between NU, NV, NW terminals and N1	<p>Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below.</p> <ul style="list-style-type: none"> HVIC malfunction by VS voltage (output terminal potential) decreasing excessively. LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	The cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIM. Then since the incorrect signals are input to DIPIM, the arm short circuit might occur.

3.1.8 SOA of DIIPM

The following describes the SOA (Safety Operating Area) of DIIPM.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: The total amount of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(prot)}$: DC-link voltage that DIIPM can protect itself.

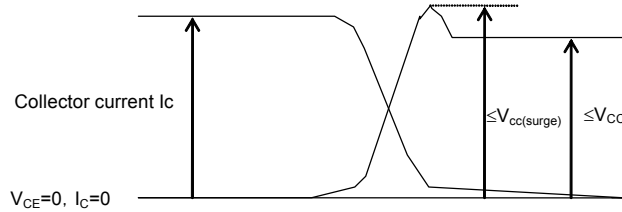


Fig.3-11 SOA at switching mode

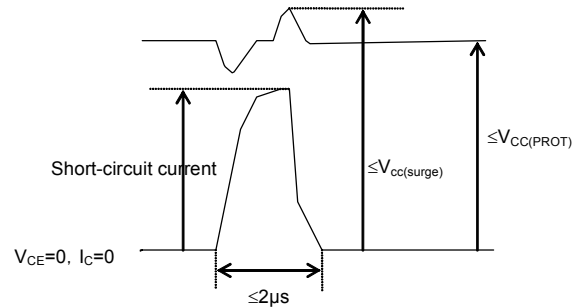


Fig.3-12 SOA at short-circuit mode

In Case of switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC} , that is 450V.

In Case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC} , that is, 400V.

3.1.9 SCSOA

Fig.3-13 and Fig.3-14 show the typical SCSOA performance curves of PS21A7A and PS21A79.

Conditions: $V_{CC}=400V$, $T_j=125^{\circ}C$ at initial state, $V_{CC(surge)} \leq 500V$ (surge included), non-repetitive, 2m load.

The DIIPM can shutdown safely an SC current that is about 10 times of its current rating under the conditions only if the IGBT conducting period is less than 4.5μsec.

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

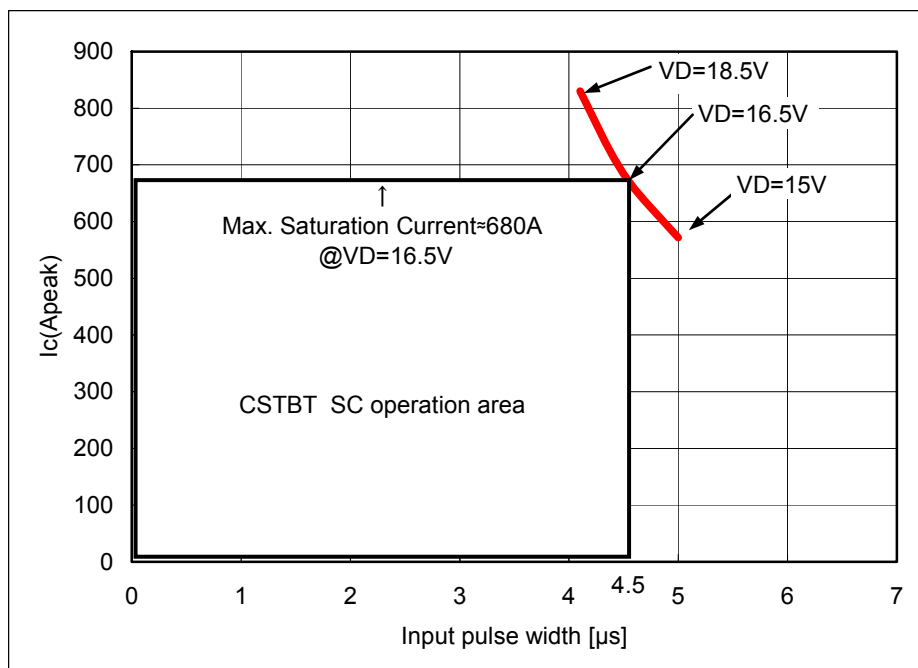


Fig.3-13 PS21A7A typical SCSOA curve

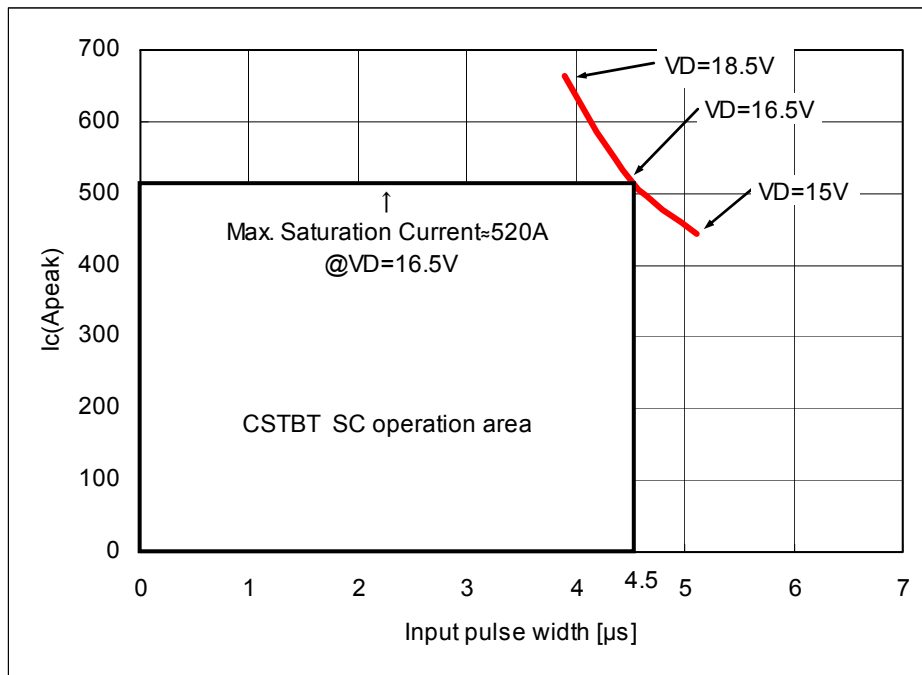


Fig.3-14 PS21A79 typical SCSOA curve

3.1.10 Power Life Cycles

When DIIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔT_j). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-15 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔT_j).

(The curve is a regression curve based on 3 points of $\Delta T_j = 46, 88, 98^\circ\text{C}$ with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

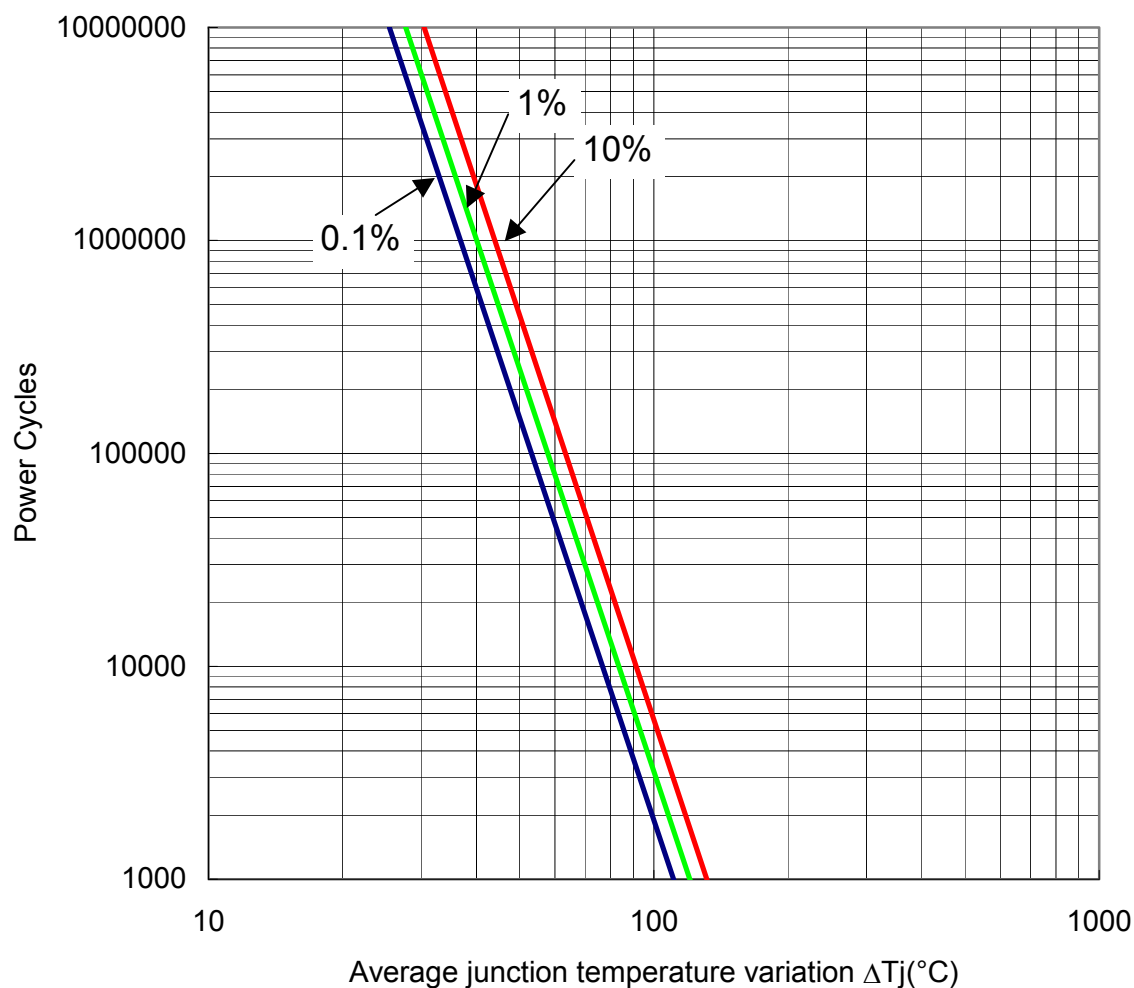


Fig.3-15 Power cycle curve



3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- Assumptions

- (1) PWM controlled VVVF inverter with sinusoidal output;
- (2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
- (3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
- (4) Output current varies with $I_{cp} \times \sin x$ and it does not include ripple.
- (5) Power factor of load output current is $\cos\theta$, ideal inductive load is used for switching.

- Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+D \times \sin x}{2}$ which is equivalent to the output voltage variation. From the power factor $\cos\theta$, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$\text{Output current} = I_{cp} \times \sin x$$

$$\text{PWM Duty} = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$V_{ce(sat)} = V_{ce(sat)} (@ I_{cp} \times \sin x)$$

$$V_{ec} = (-1) \times V_{ec} (@ I_{cp} (= I_{cp}) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi} \int_0^\pi (I_{cp} \times \sin x) \times V_{ce(sat)} (@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi} \int_\pi^{2\pi} ((-1) \times I_{cp} \times \sin x) ((-1) \times V_{ec} (@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi} \int_0^\pi (P_{sw(on)} (@ I_{cp} \times \sin x) + P_{sw(off)} (@ I_{cp} \times \sin x)) \times f_c \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-16, and its dynamic loss can be calculated by the following expression:

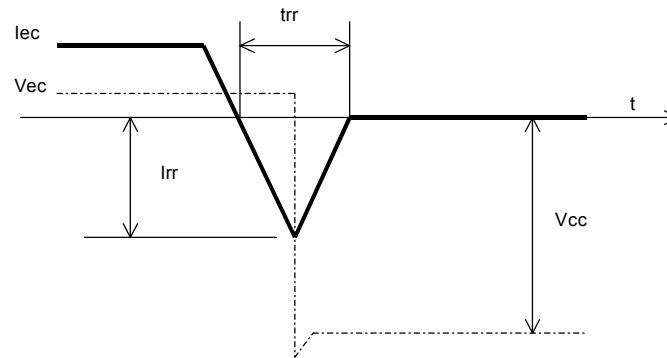


Fig.3-16 Ideal FWDi recovery characteristics curve

$$P_{sw} = \frac{I_{rr} \times V_{cc} \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\begin{aligned} & \frac{1}{2} \int_{\pi}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times trr(@ I_{cp} \times \sin x)}{4} \times fc \bullet dx \\ &= \frac{1}{8} \int_{\rho}^{2\pi} I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times trr(@ I_{cp} \times \sin x) \times fc \bullet dx \end{aligned}$$

● Attention of applying the power loss simulation for inverter designs

- Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC} , and P_{sw} corresponding to the output current. The worst condition is most important.
- PWM duty depends on the signal generating way.
- The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
- $V_{CE(sat)}$, V_{EC} and $P_{sw}(on, off)$ should be the values at $T_j=125^{\circ}\text{C}$.



3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-17 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: $V_{CC}=300V$, $V_D=V_{DB}=15V$, $V_{CE(sat)}=Typ.$, $P.F=0.8$, Switching loss=Typ., $T_j=125^{\circ}C$, $T_c=100^{\circ}C$, $R_{th(j-c)}=Max.$, 3-phase PWM modulation, 60Hz sine waveform output

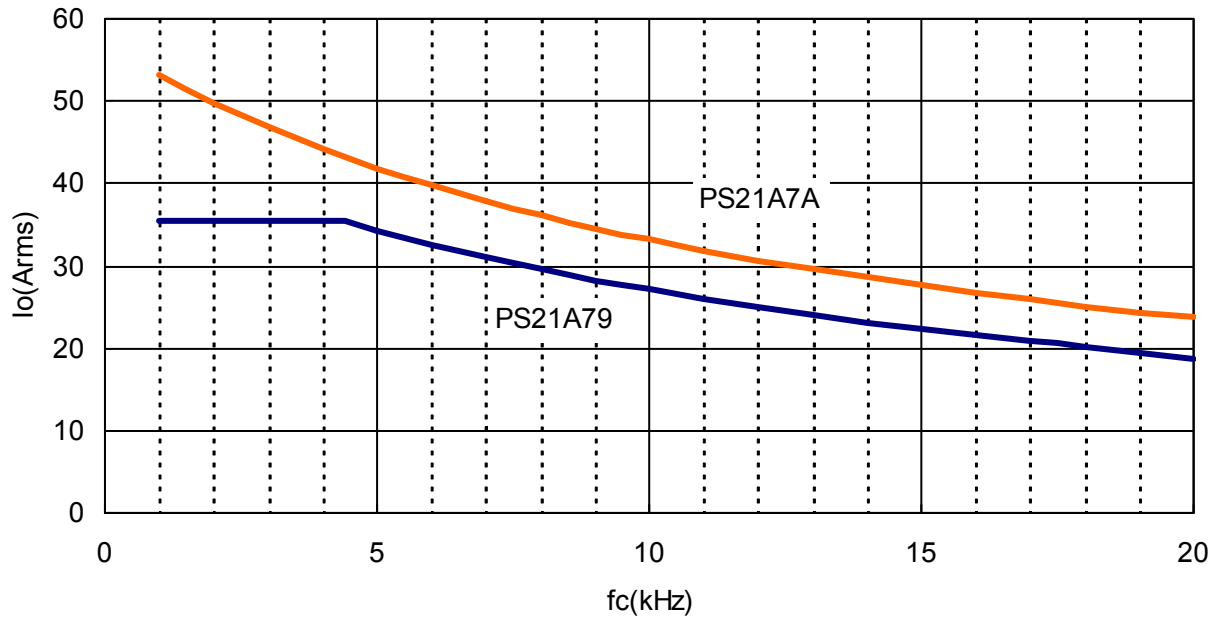


Fig.3-17 Effective current-carrier frequency characteristic

Fig.3-17 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition ($T_c=100^{\circ}C$ and $T_j=125^{\circ}C$). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided by Mitsubishi electric on its web site (URL: <http://www.mitsubishichips.com/>).

3.3 Noise Withstand Capability

3.3.1 Evaluation Circuit

DIIPM have been confirmed to be with over $\pm 2.0\text{kV}$ noise withstand capability by the noise evaluation under the conditions shown in Fig.3-18. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

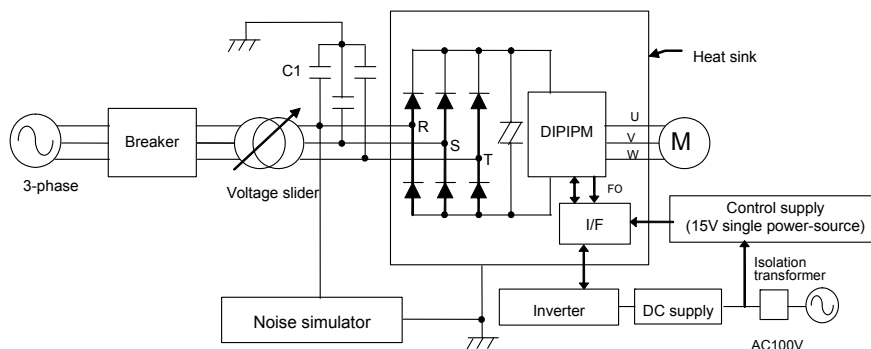


Fig.3-18 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers
15V single power supply, Test is performed with IM

Test conditions

$V_{CC}=300\text{V}$, $V_D=15\text{V}$, $T_a=25^\circ\text{C}$, no load

Scheme of applying noise: From AC line (R, S, T), Period $T=16\text{ms}$, Pulse width $t_w=0.05\text{--}1\mu\text{s}$, input in random.

3.3.2 Countermeasures and Precautions

DIIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIIPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

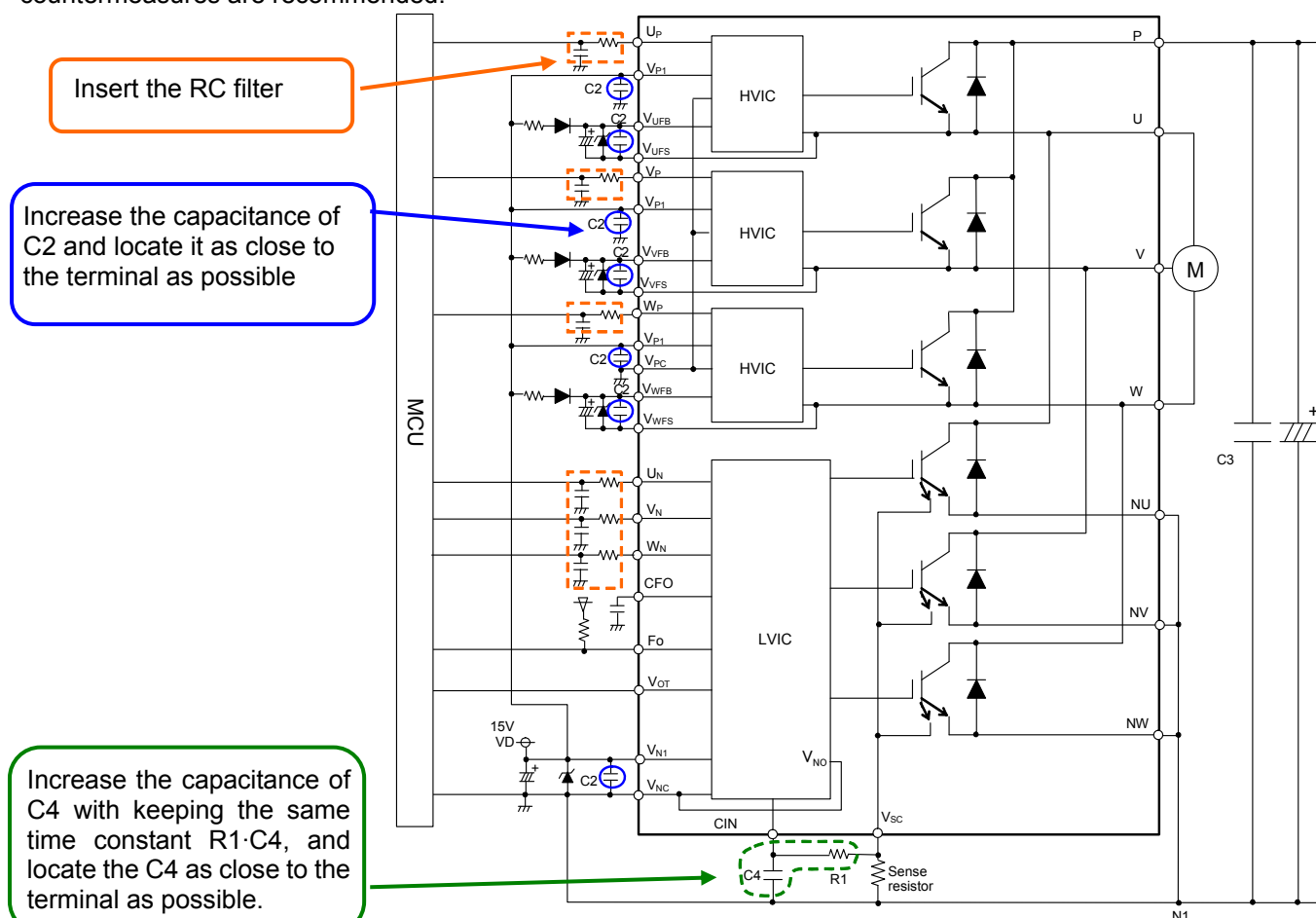


Fig.3-19 Example of countermeasures

3.3.3 Static Electricity Withstand Capability

DIIPM has been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-20 and Fig.3-21. The results (typical data) are described in Table 3-4

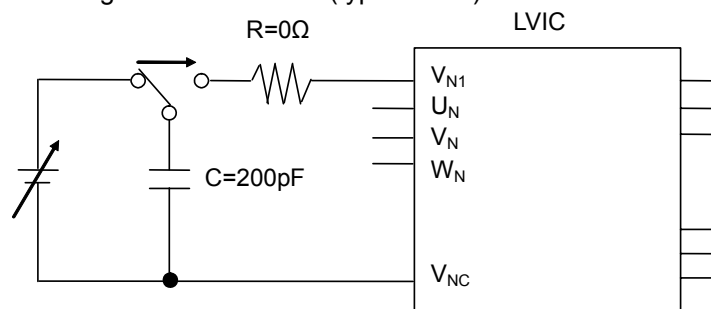


Fig.3-20 V_{N1} terminal Surge Test circuit

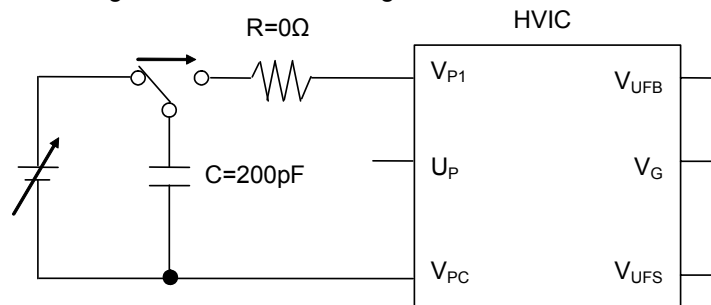


Fig.3-21 V_{P1} terminal Surge Test circuit

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage.
(Limit voltage of surge simulator: $\pm 4.0\text{kV}$, Judgment method; change in V-I characteristic)

Table 3-4 Typical ESD capability for PS21A7A and PS21A79

[Control terminal part]

For control part, since both have same circuit in the control IC, they have same capability.

Terminals	+	-
UP, VP, WP- V_{NC}	1.6	1.7
$V_{P1} - V_{NC}$	3.6	3.7
$V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	4.0 or more	4.0 or more
UN, VN, WN- V_{NC}	0.7	1.6
$V_{N1}-V_{NC}$	4.0 or more	4.0 or more
CIN- V_{NC}	0.8	1.0
FO- V_{NC}	1.5	2.4
CFO- V_{NC}	1.3	1.7
$V_{OT}-V_{NC}$	0.9	2.5

[Power terminal part for PS21A7A]

Terminals	+	-
$V_{SC}-V_{NC}^*$	0.4	0.5
P—NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS21A79]

Terminals	+	-
$V_{SC}-V_{NC}^*$	0.5	1.1
P—NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

* V_{SC} terminal (IGBT sense) is connected to the power chip inside the module.

CHAPTER4 KEY PARAMETERS SELECTING GUIDANCE

4.1 Single Supply Drive Scheme

4.1.1 Bootstrap Capacitor Initial Charging

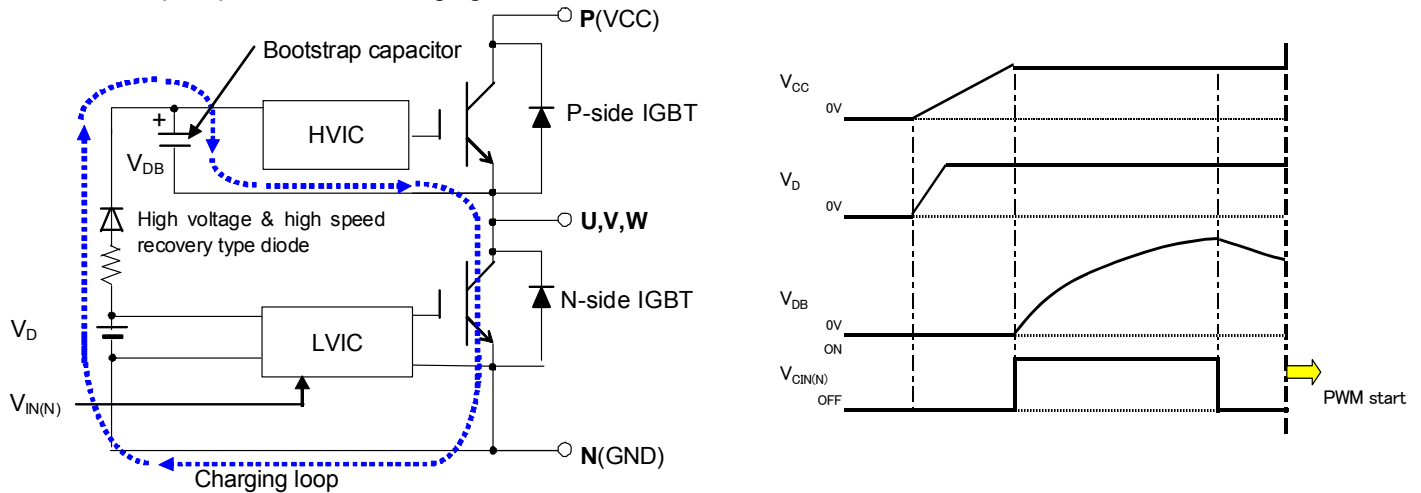


Fig.4-1 Initial charging loop and timing chart of bootstrap circuit

By using bootstrap circuit, conventional three isolated 15V power supply for P-side three IGBT drive can be eliminated. The initial charge of the bootstrap capacitors is necessary to start-up the inverter. Fig.4-2 shows the charge mechanism. The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.

For reference, the charging time for the bootstrap circuit with a 100μF capacitor and 50Ω current limiting resistor is about 5msec.

4.1.2 Charging and Discharging of the Bootstrap Capacitor During Inverter Operation

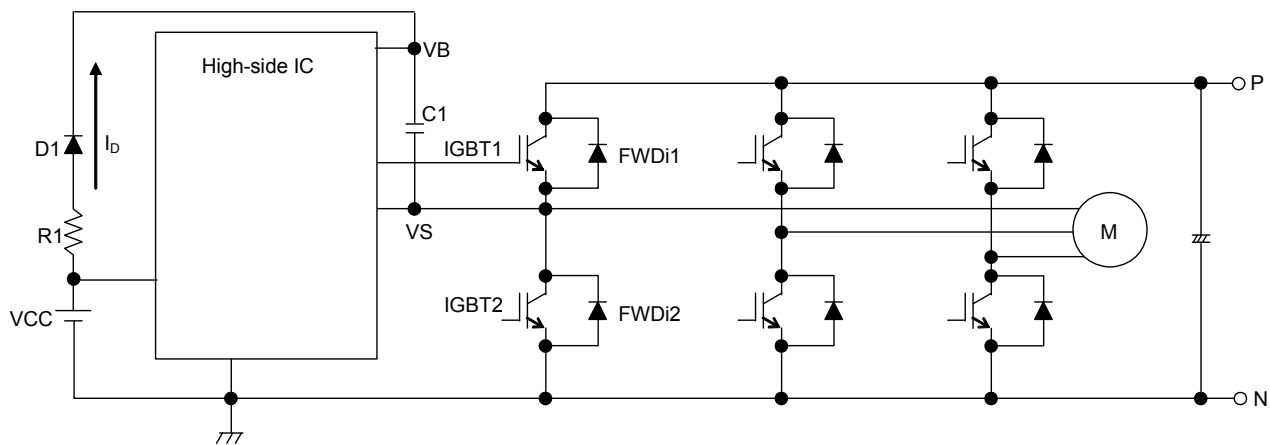


Fig.4-2 Inverter circuit diagram

(1) Charging operation Timing Chart of Bootstrap Capacitor (C1)

Sequence (1-1) : IGBT2 ON (Fig.4-3)

When IGBT2 is in ON state, charging voltage on C1 ($V_{C(1)}$) is calculated by

$$V_{C(1)} = V_{CC} - V_{F1} - V_{sat2} - I_D \cdot R1 \quad (\text{Transient state})$$

$$V_{C(1)} = V_{CC} \quad (\text{Steady state})$$

where V_{CC} is the charging supply voltage, V_{F1} the forward voltage drop of diode D1, V_{sat2} the saturation voltage of IGBT2, I_D the charging current, and R1 the inrush current limitation resistance.

Then, IGBT2 is turned off. Motor current will flow through the free-wheel path of FWDi1. Once the electric potential of VS rises near to that of P, the charging to C1 is stopped.

When IGBT1 is in ON state, the voltage of C1 gradually declines from the potential $V_{C(1)}$ due to the current consumed by the drive circuit.

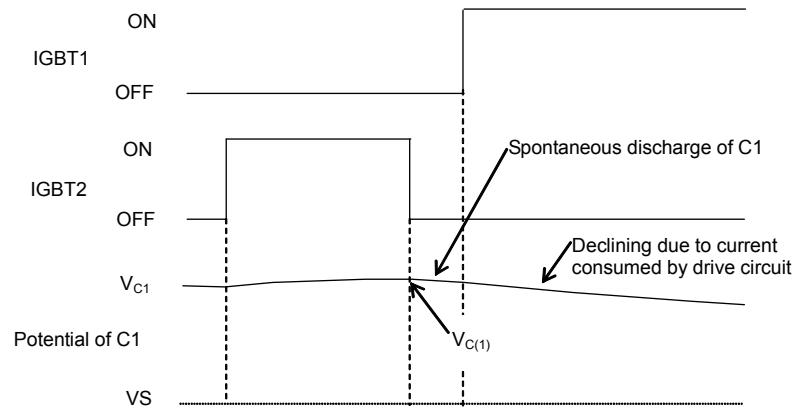


Fig.4-3 Timing chart of sequence (1-1)

Sequence (1-2): IGBT2 OFF and FWDi2 ON (Fig.4-4)

When IGBT2 is OFF and FWDi2 is ON, the voltage on C1 (V_{C(2)}) is calculated by:

$$V_{C(2)} = V_{CC} - V_{F1} + V_{EC2}$$

where V_{EC2} denotes the forward voltage drop of FWDi2.

When both IGBT2 and IGBT1 are OFF, the regenerative current flows continuously through the free-wheel path of FWDi2. Therefore the potential of V_S drops to -V_{EC2}, then C1 is recharged to restore the declined potential. When IGBT1 is turned ON, the potential of V_S rises to that of P, the charge to C1 stops and the voltage on C1 gradually declines from the potential V_{C(2)} due to the current consumed by the drive circuit.

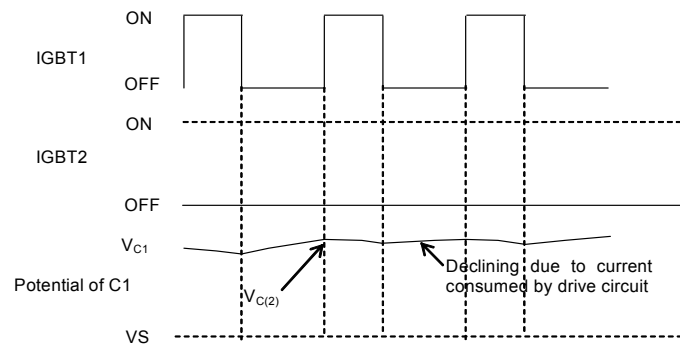


Fig.4-4 Timing chart of sequence (1-2)

(2) Instruction of Selecting the Bootstrap Capacitor (C1) and Resistance (R1)

The capacitance of bootstrap capacitor can be calculated by:

$$C1 = I_{BS} \times T1 / \Delta V$$

where T1 is the maximum ON pulse width of IGBT1 and I_{BS} is the drive current of the IC (depends on temperature and frequency characteristics), and ΔV is the allowable discharge voltage. A certain margin should be added to the calculated capacitance.

Resistance R1 should be basically selected such that the time constant C1R1 will enable the discharged voltage (ΔV) to be fully charged again within the minimum ON pulse width (T2) of IGBT2.

However, if only IGBT1 has an ON-OFF-ON control mode (Fig.4-5), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

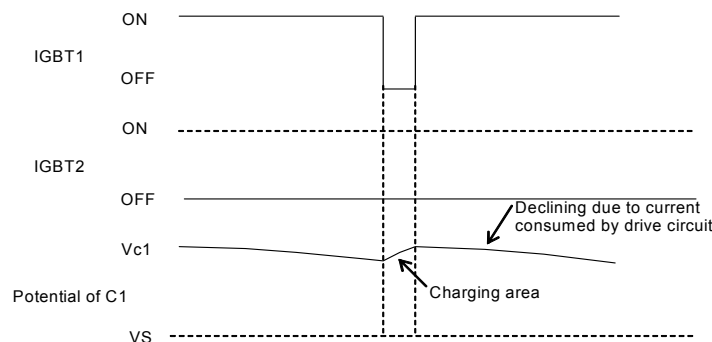


Fig.4-5 Timing Chart of ON-OFF-ON Control Mode

Design example of Bootstrap circuit

■ Selecting bootstrap capacitor

Suppose ΔV_{DB} (discharged voltage)=1V, the maximum ON pulse width T1 of P-side IGBT is 5msec, and I_{DB} is 0.55mA(Max. rating), then

$$C = I_{DB} \times T1 / \Delta V_{DB} = 2.75 \times 10^{-6}$$

the calculated bootstrap capacitance is 2.75 μ F. By taking consideration of dispersion and reliability, the capacitance is generally selected as large as 2~3 times of the calculated one, for example, 10 μ F or above for this case is suitable.

■ Selecting bootstrap resistor

Suppose the bootstrap capacitance is 10 μ F, V_D =15V, V_{DB} =14V, and the minimum ON pulse width t_0 of N-side IGBT (or the minimum OFF pulse width t_0 of upper-side IGBT) is 20 μ s, then to recover V_{DB} to 15V during this period, the bootstrap resistance should be

$$R = \{(V_D - V_{DB}) \times t_0\} / (C \times \Delta V_{DB}) = 2$$

This means a 2 Ω resistor is suitable.

Note:

- (1) In the case of the control for DCBLM or 2-phase modulation for IM (Induction Motor), there will be a long ON time period on the P-side IGBT, please pay attention to the bootstrap supply voltage drop.
- (2) The above result is only a calculation example. It is recommended to design a system by taking consideration of the actual control pattern and lifetime of components.

For reference, Fig.4-6 and 4-7 are the circuit current I_{DB} for P-side IGBT driving supply (V_{DB}) vs. carrier frequency characteristics (@ V_D = V_{DB} =15V, T_j =125°C, IGBT ON Duty=10, 30, 50, 70, 90%)

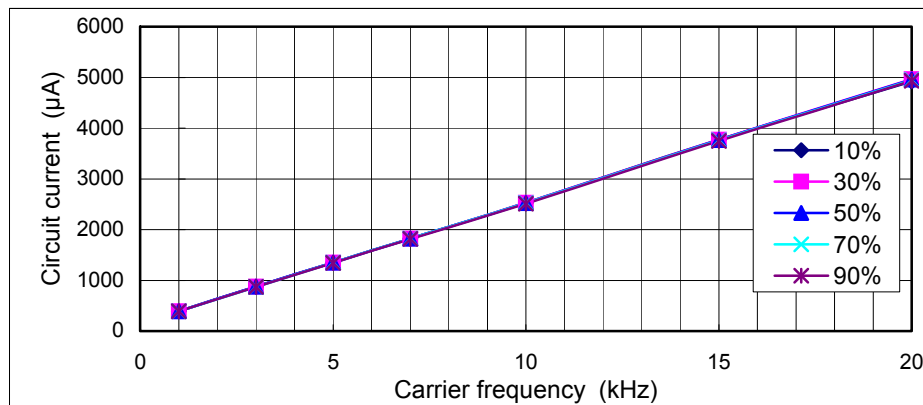


Fig.4-6 I_{DB} vs. Carrier frequency for PS21A7A

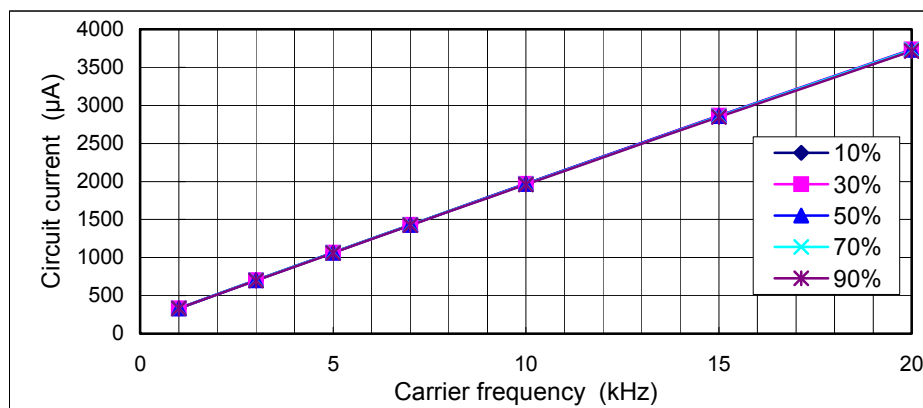


Fig.4-7 I_{DB} vs. Carrier frequency for PS21A79

■ Selecting bootstrap diode

The bootstrap diode with blocking voltage over 600V is recommended. In DIIPM, the maximum rating of power supply is 450V. The actual voltage applied on the diode is 500V by adding a surge voltage of about 50V. Furthermore, if considering 100V for the margin, 600V class diode is necessary. The diode is also highly recommended to be with fast recovery characteristics (recovery time less than 100nsec).

■ Noise filter for control supply

It is recommended to insert a film type or ceramic type noise filter with 0.22-2 μ F to the control supply terminals ($V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$, $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$). The smaller the supply parasitic impedance is, the smaller a feasible noise filter capacitance can be. The supply circuit should be such designed that the noise fluctuation is less than $\pm 1V/\mu s$, and the ripple voltage is less than $\pm 2V$.

Reference:

There are two kinds of control supply in general use. The first one is DC-DC converter (3-terminal regulator), of which input DC supply comes from AC-transformer. The other is DC-DC converter (switching regulator), of which input DC supply is generated by a SMPS.

Note:

After bootstrap capacitor voltage has been fully charged, input one pulse in the P-side input signals to reset internal IC state before starting formal PWM.



CHAPTER5 PACKAGE HANDLING

5.1 Packaging Specification

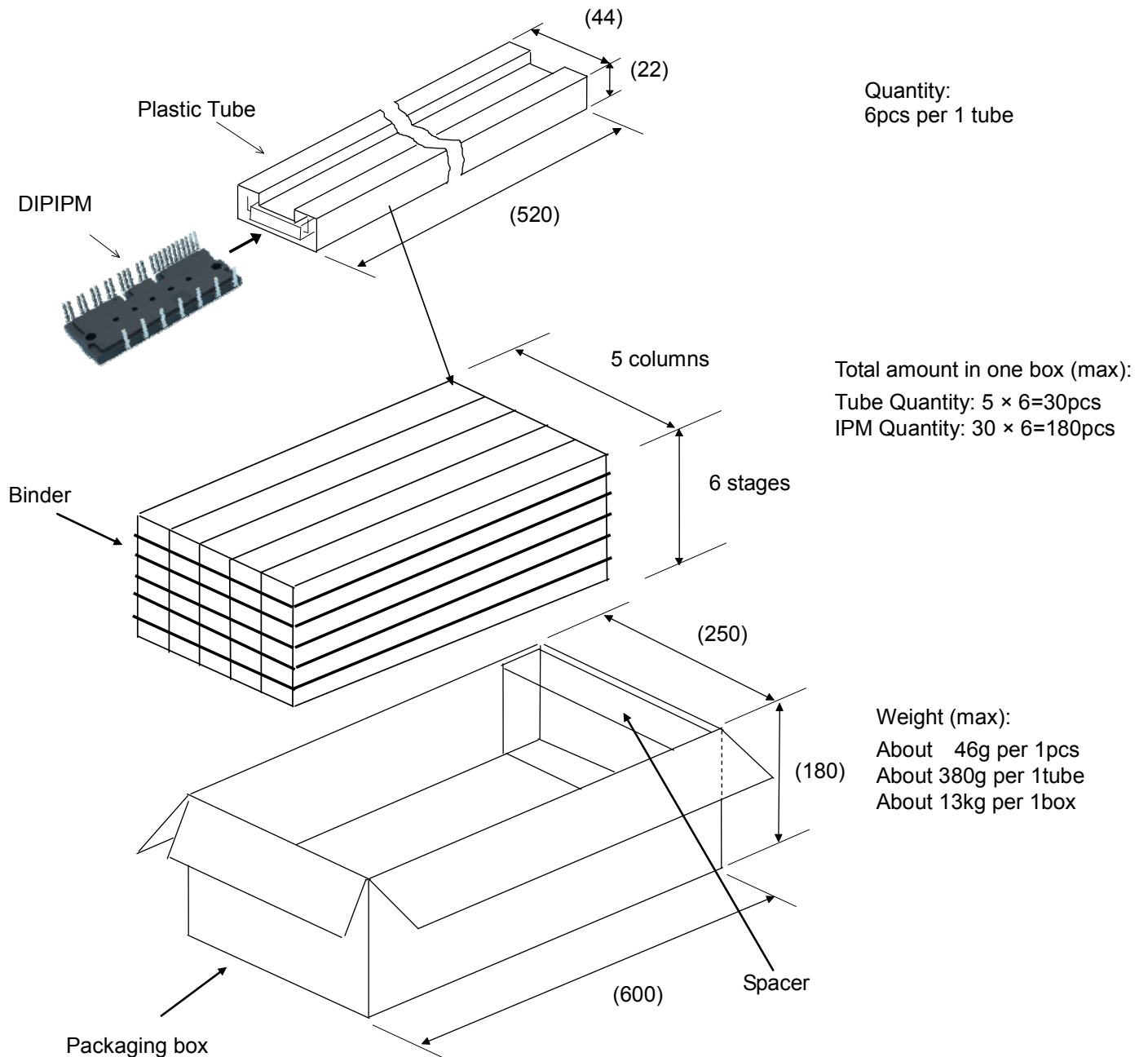


Fig.5-1 Packaging Specification

5.2 Handling Precautions

Cautions

Transportation	<ul style="list-style-type: none"> •Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. •Throwing or dropping the packaging boxes might cause the devices to be damaged. •Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	<ul style="list-style-type: none"> •We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	<ul style="list-style-type: none"> •When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	<ul style="list-style-type: none"> •Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	<ul style="list-style-type: none"> •The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	<ul style="list-style-type: none"> •ICs and power chips with MOS gate structure are used for the DIIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. <p>(1)Precautions against the device destruction caused by the ESD</p> <p>The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.</p> <ul style="list-style-type: none"> *Containers that charge static electricity easily should not be used for transit and for storage. *Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. *Should not be taking out DIIPM from tubes until just before using DIIPM and never touch terminals with bare hands. *During assembly and after taking out DIIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. *When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. *If using a soldering iron, earth its tip. <p>(2)Notice when the control terminals are open</p> <ul style="list-style-type: none"> *When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. *Short the terminals before taking a module off.

Keep safety first in your circuit designs!

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Appendix Revision Record

Revision	Page No.	Content
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