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LARGE DIPIPM Ver.4

APPLICATION NOTE

PS22A7* series

MITSUBISHI ELECTRIC CORPORATION
POWER DEVICE WORKS

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CHAPTER1 INTRODUCTION

1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

1.2 Product Line-up

Table 1-1. Line-up

Type Name	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
PS22A72	5A/1200V	0.75kW/440VAC	V_{iso} = 2500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS22A73	10A/1200V	1.5kW/440VAC	
PS22A74	15A/1200V	2.2kW/440VAC	
PS22A76	25A/1200V	3.7kW/440VAC	
PS22A78-E	35A/1200V	5.5kW/440VAC	

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

1.3 Functions and Features

1200V Large DIPIPM Ver.4 is a compact intelligent power module with transfer mold package favorable for larger mass production. And it includes power chips, drive and protection circuits.

One of the most important features of 1200V Large DIPIPM Ver.4 is that it realized higher thermal dissipation by incorporating high thermal conductive structure with insulated sheet, so that the chip shrink became possible and achieved higher current rating (35A) than previous 1200V Large DIPIPM series (25A/1200V), despite its mounting area decreases to 75%.

In addition, since 600V rating series are available with same package and pin layout, it is able to use the same designed PCB.

Fig.1-1, Fig.1-2 and Fig.1-3 show the outline photograph, internal cross-section structure and the circuit block diagram respectively.

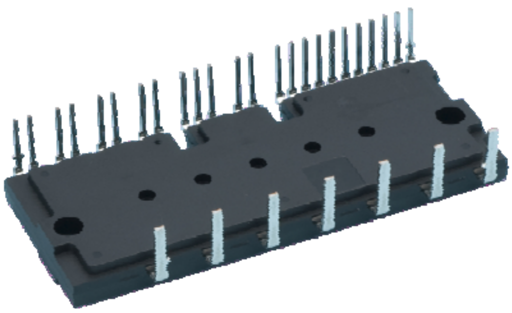


Fig.1-1 Package photograph

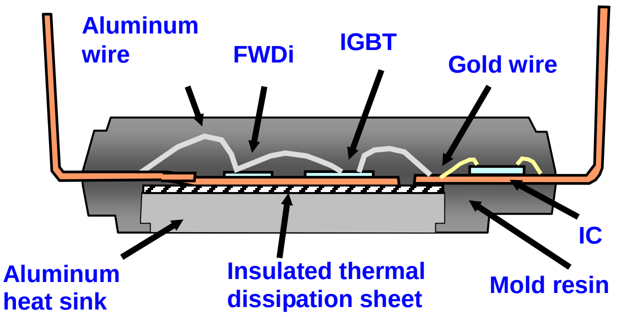


Fig.1-2 Internal cross-section structure

Features:

- For P-side IGBTs
  - -Drive circuit
  - -High voltage level shift circuit
  - -Control supply under voltage (UV) protection circuit (without fault signal output)
- For N-side IGBTs
  - -Drive circuit
  - -Short circuit (SC) protection circuit (by using external current detecting resistor)
  - -Control supply under voltage (UV) protection circuit (with fault signal output)
  - -Analog output of LVIC temperature
- Fault Signal Output
  - -Corresponding to SC protection and N-side UV protection
- IGBT Drive Supply
  - -Single DC15V power supply
- Control Input Interface
  - -High active logic

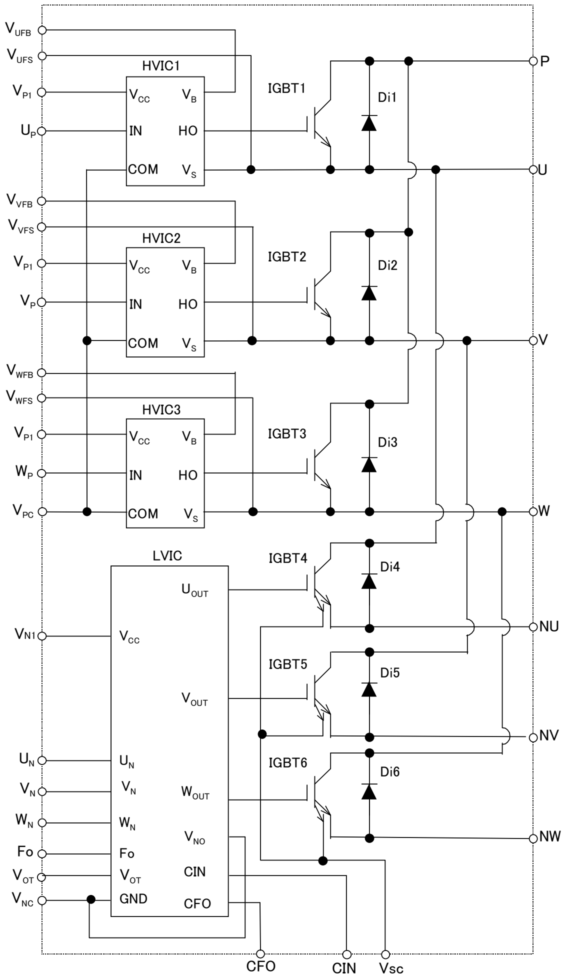


Fig.1-3 Internal circuit schematic

1.4 The differences of previous series (1200V Large DIPIPM PS2205*) and this series

(1) Enlargement of maximum current rating to 35A

Due to change its insulation structure from mold resin insulation to insulated thermal dissipation sheet, it became possible to decrease the thermal resistance between junction and case Rth(j-c) substantially. So that despite its mounting area decreases to 75%, it realized higher current rating up to 35A than previous 1200V Large DIPIPM.

(2) Changing the method of short circuit protection (SC)

In the previous series the shunt resistor was inserted between N terminal and power GND line for detecting short circuit current. But the loss at the resistor escalates with increasing current rating, so high wattage type resistor is needed. In this series, the current detection method was changed to the one of detecting slight sense current divided from main current by using on-chip current sense IGBTs. So that the shunt resistor inserted to main flow path for SC protection is unnecessary. For more detail, refer Section 2.2.1.

(3) Analog output function of LVIC temperature

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC and output it by analog signal. But the heat generated at IGBT and FWDi transfers to LVIC through the mold package and the inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)

It is able to replace the thermistor which was set on outer heat sink currently.

For more detail, refer Section 2.2.3.

(4) Terminal layout

Because of above (2), (3) functions addition and divided N-side IGBT emitter, the terminal layout was changed from 1200V Large DIPIPM series.

For more detail, refer Section 2.3.

CHAPTER2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Specifications

The specifications are described below by using PS22A78-E (35A/1200V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS22A78-E are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS22A78-E

Maximum Ratings (Tj=25°C, unless otherwise noted):

Inverter Part:

Item	Symbol	Condition	Rating	Unit	
Supply voltage	V_{CC}	Applied between P-NU,NV,NW	900	V	(1)
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-NU,NV,NW	1000	V	(2)
Collector-emitter voltage	V_{CES}		1200	V	(3)
Each IGBT collector current	$\pm I_C$	Tc=25°C	35	A	(4)
Each IGBT collector current (peak)	$\pm I_{CP}$	Tc=25°C, less than 1ms	70	A	
Collector dissipation	P_C	Tc=25°C, per 1 chip	129.9	W	
Junction temperature	T_j		-20~+150	°C	(5)

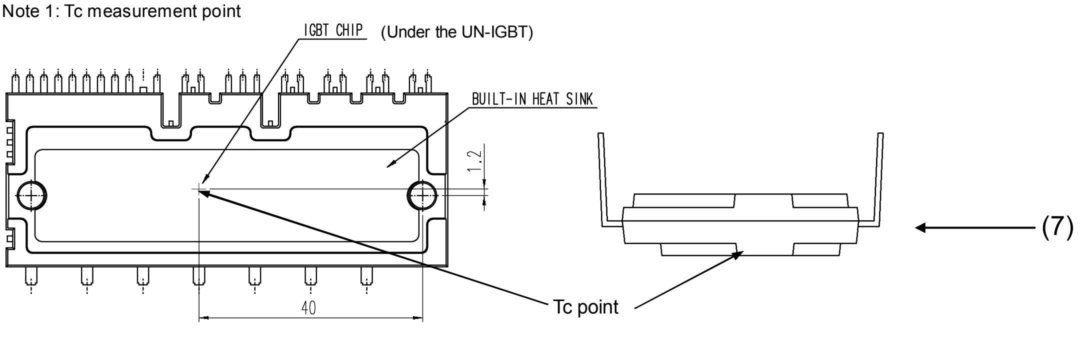
Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between V_{P1}-V_{PC},V_{N1}-V_{NC}	20	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS} ,V_{WFB}-V_{WFS}	20	V
Input voltage	V_{IN}	Applied between U_P,V_P,W_P-V_{PC}, U_N,V_N,W_N-V_{NC}	-0.5~V_D+0.5	V
Fault output supply voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5~V_D+0.5	V
Fault output current	I_{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

Total System

Item	Symbol	Condition	Rating	Unit	
Self protection supply voltage limit (short circuit protection capability)	$V_{CC(PROT)}$	V_D=13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	800	V	(6)
Module case operation temperature	Tc	(Note 1)	-20~+100	°C	
Storage temperature	Tstg		-40~+125	°C	
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	Vrms	

Note 1: Tc measurement point



[Item explanation]

(1) Vcc — The maximum P-N voltage in no switching state. A voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.

(2) Vcc(surge) — The maximum P-N surge voltage in switching state. A snubber circuit is necessary if the voltage exceeds Vcc(surge).

(3) V_{CES} — The maximum sustained collector-emitter voltage of built-in IGBT.

(4) $\pm I_C$ — The allowable DC current continuously flowing at collect electrode (@Tc=25°C)

(5) Tj — The maximum junction temperature rating is 150°C.But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetive temperature variation ΔTj affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.

(6) Vcc(prot) — The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.

(7) Tc position — Tc (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance of PS22A78-E.

Table 2-2. Thermal resistance of PS22A78-E

Thermal Resistance :

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	-	-	0.77	°C / W
	$R_{th(j-c)F}$	Inverter FWD part (per 1/6 module)	-	-	1.25	

(Note 2) Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10sec is called as transient thermal impedance which is shown in Fig.2-1. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max) For example, the IGBT transient thermal impedance of PS22A78-E in 0.1s is 0.77×0.5=0.39K/W.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (e.g. In the cases at motor starting, at motor lock･･･)

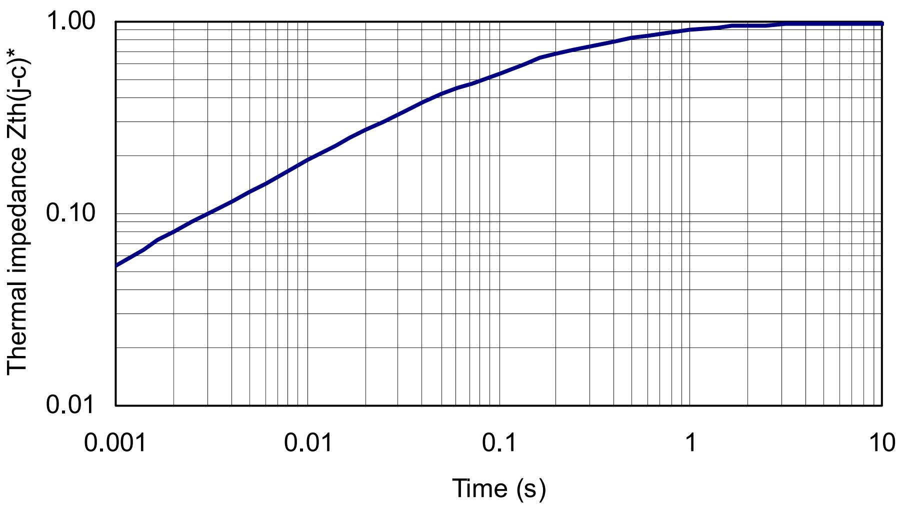


Fig.2-1 Typical transient thermal impedance

2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics of PS22A78-E.

Table 2-3. Static characteristics and switching characteristics of PS22A78-E

Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_D=V_{DB}=15V V_{IN}=5V, I_C=35A,	Tj=25°C	-	1.9	2.6	V
			Tj=125°C	-	2.0	2.7	
FWDi forward voltage	V_{EC}	V_{IN}=0V, -I_C=35A		-	2.2	2.8	V
Switching time	t_{on}	V_{CC}=600V, V_D=V_{DB}=15V I_C=35A, V_{IN}=0-5V Tj=125°C Inductive load		0.5	1.2	1.9	μs
	t_{rr}			-	0.5	-	
	$t_{c(on)}$			-	0.6	0.9	
	t_{off}			-	2.4	3.5	
	$t_{c(off)}$			-	0.6	0.9	
Collector-emitter cut-off current	I_{CES}	V_{CE}=V_{CES}	Tj=25°C	-	-	1	mA
			Tj=125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

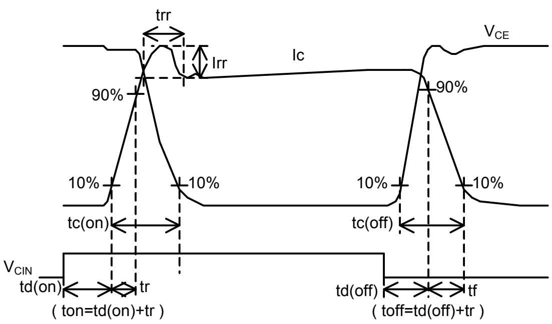


Fig.2-2 Switching time definition

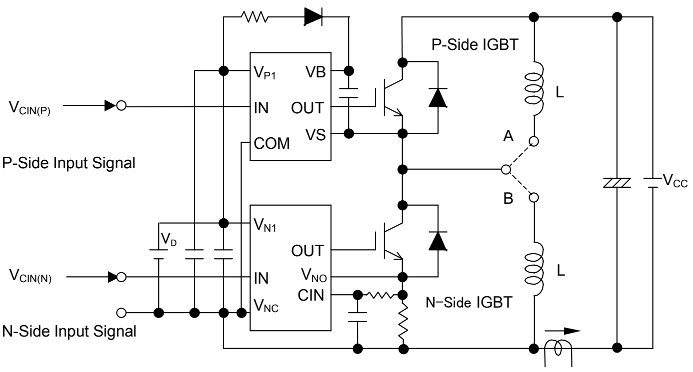


Fig.2-3 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation

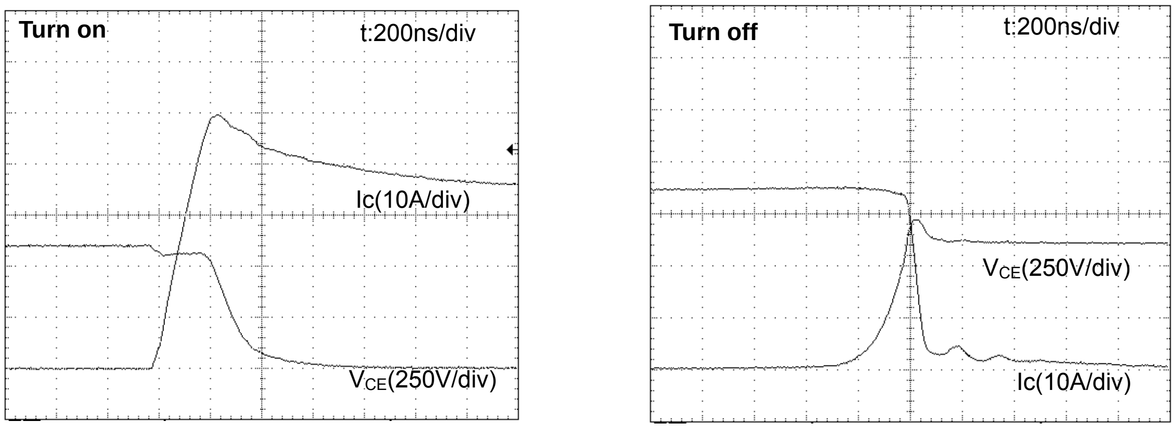


Fig.2-4 Typical switching waveform (PS22A78-E)
Conditions : V_{CC}=600V, V_D=V_{DB}=15V, Tj=125°C, Ic=35A, Inductive load half-bridge circuit

2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PS22A78-E

Control (Protection) Part :

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	V_D=V_{DB}=15V V_{IN}=5V	Total of V_{P1}-V_{PC},V_{N1}-V_{NC}	-	-	5.60	mA
			V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	1.10	
		V_D=V_{DB}=15V V_{IN}=0V	Total of V_{P1}-V_{PC},V_{N1}-V_{NC}	-	-	5.60	
			V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	-	-	1.10	
Fo output voltage	V_{FOH}	Vsc=0V, Fo terminal pull-up to 5V by 10kΩ		4.9	-	-	V
	V_{FOL}	Vsc=1V, I_{FO}=1mA		-	-	0.95	
Input current	I_{IN}	V_{IN}=5V		0.7	1.0	1.5	mA
Short circuit trip level (Note 3)	I_{SC}	-20°C≤Tc≤100°C, Rs=48.7Ω (±1%), Not connecting outer shunt resistors to NU,NV,NW terminals		59.5	-	-	A
Control supply under-voltage protection	UV_{DBt}	Tc≤100°C	Trip level	10.0	-	12.0	V
	UV_{DBr}		Reset level	10.5	-	12.5	
	UV_{Dt}		Trip level	10.3	-	12.5	
	UV_{Dr}		Reset level	10.8	-	13.0	
Fault output pulse width	t_{FO}	C_{FO}=22nF (Note 4)		1.6	2.4	-	ms
ON threshold voltage	Vth(on)	Applied between U_P,V_P,W_P-V_{PC}, U_N,V_N,W_N-V_{NC}		-	-	3.5	V
OFF threshold voltage	Vth(off)			0.8	-	-	
Temperature output	V_{OT}	At LVIC temperature=85°C (Note 5)		3.57	3.63	3.69	V

(Note 3) Short circuit (SC) protection is functioning only for N-side IGBTs.
(Note 4) Fault signal is output when the lower arms short circuit or control supply under-voltage protective functions operate.
The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO}. (t_{FO}(typ)= C_{FO} / (9.1 × 10^{-6}) [s])
(Note 5) DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively.
When temperature exceeds the protect level that customer defined, controller (MCU) should stop the DIPIPM.

2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS22A78-E are given in Table 2-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

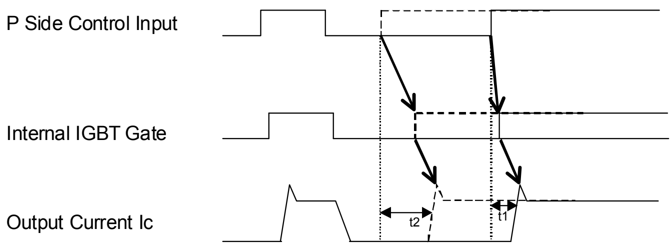
Table 2-5 Recommended operating conditions of PS22A78-E

Recommended Operation Conditions :

Item	Symbol	Condition		Recommended Min.	Recommended Typ.	Recommended Max.	Unit
Supply voltage	V_{CC}	Applied between P-NU,NV,NW		350	600	800	V
Control supply voltage	V_D	Applied between V_{P1}-V_{PC},V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
Control supply variation	ΔV_D,ΔV_{DB}			-1	-	+1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, $T_C \le 100°C$		3.0	-	-	μs
PWM input frequency	f_{PWM}	$T_C \le 100°C$, $T_j \le 125°C$		-	-	20	kHz
Output rms current	I_O	V_{CC}=600V, V_D=15V P.F=0.8 Sinusoidal PWM, $T_C \le 100°C$, $T_j \le 125°C$ (Note 7)	f_{PWM}=5kHz	-	-	19.1	A_{rms}
			f_{PWM}=15kHz	-	-	12.8	
Minimum input pulse width	PWIN(on)	(Note 8)		1.5	-	-	μs
	PWIN(off)	$350 \le V_{CC} \le 800V$, $13.5 \le V_D \le 16.5V$, $13.0 \le V_{DB} \le 18.5V$, $-20 \le T_C \le 100°C$, N line wiring inductance less than 10nH (Note 9)	$I_C \le 35A$	2.3	-	-	
			$35 < I_C \le 59.5A$	2.9	-	-	
V_{NC} variation	V_{NC}	Potential difference between V_{NC}-NU,NV,NW including surge voltage		-5.0	-	+5.0	V
Junction temperature	Tj			-20	-	125	°C

(Note 7) The allowable output rms current also depends on user application conditions.
(Note 8) Input signal with ON pulse width less than PWIN(on) might make no response.
(Note 9) IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).
Please refer below about delayed response .

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Real line: off pulse width>PWIN(off); turn on time t1
Broken line: off pulse width<PWIN(off); turn on time t2

2.1.6 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-6

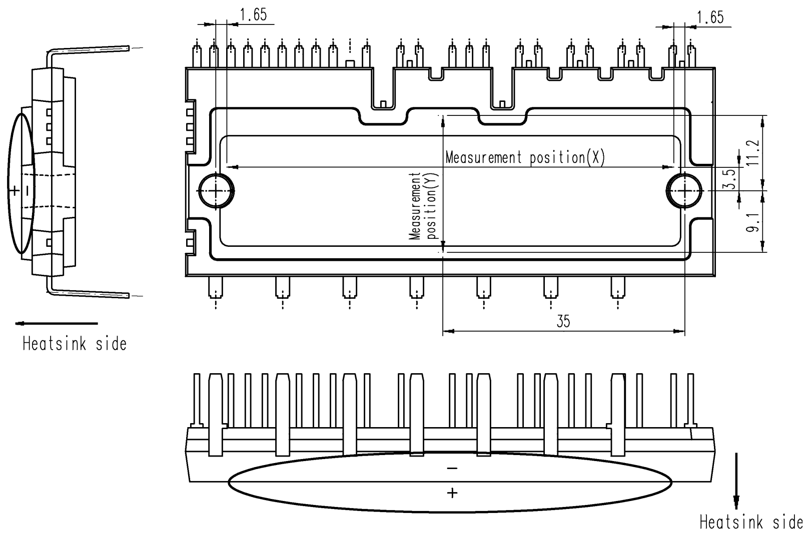
Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6 Mechanical characteristics and ratings of PS22A78-E

Mechanical Characteristics and Ratings:

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: (M4)	Recommended: 1.18N·m	0.98	–	1.47	N·m
Weight			–	46	–	g
Heat sink side flatness		(Note 6)	–50	–	100	μm

Note 6: Flatness measurement position



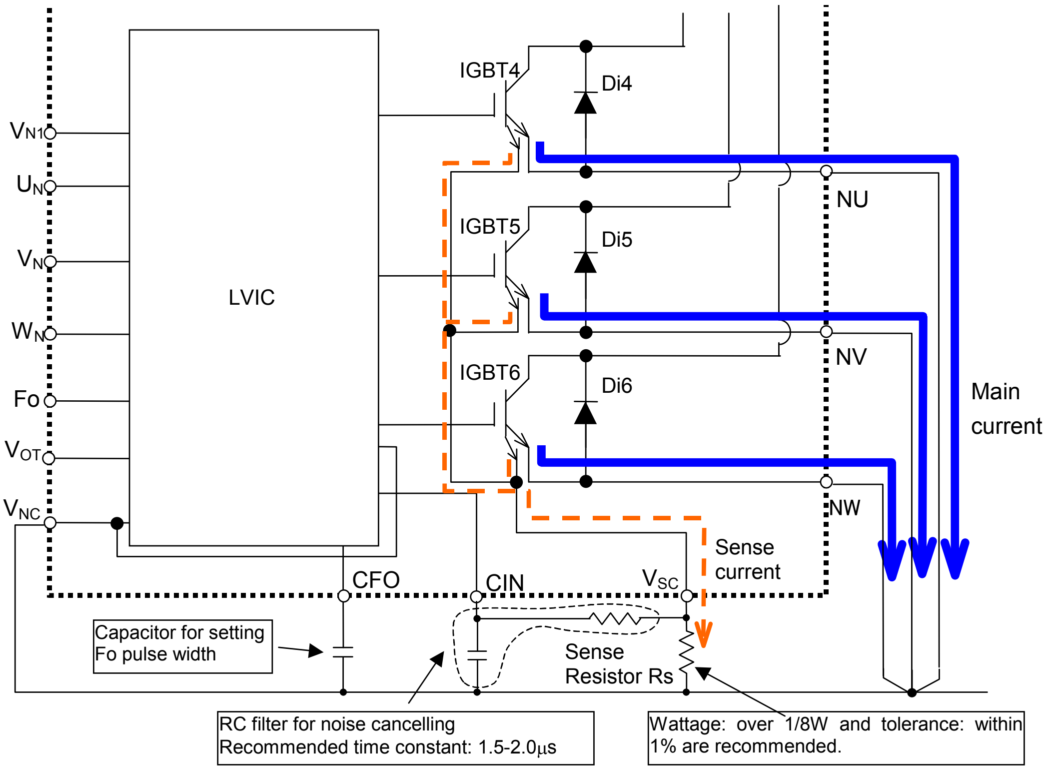
2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in the large DIPIPM Ver.4. The detailed information are described below.

2.2.1 Short Circuit Protection

In large DIPIPM Ver.4 series, the method of SC protection is different from current products, which detect main current by shunt resistor inserted into main current path.

But this SC protection detects much smaller sense current (split at N-side IGBT) by measuring the potential of sense resistor Rs, which is connected to Vsc terminal. So high wattage type shunt resistor isn't necessary for SC protection, and the loss at shunt resistor can be reduced. (Fig.2-5)



*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

Fig.2-5 SC protection circuit

SC protection works by feedback the potential, which is generated by sense current flowing into the sense resistor, to CIN terminal. And when SC ptotection occurs, DIPIPM shutdowns all N-side IGBTs hardly and outputs Fo signal. (its pulse width is set by CFO capacitor.)

To prvent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to 1.5μ-2.0μs because guranteed short circuit ptotection capability of DIPIPM is within 2μs.

Table 2-7 SC protection trip level

	Rs	Min.
PS22A78-E	48.7Ω	59.5A
PS22A76	82.5Ω	42.5A
PS22A74	82Ω	25.5A
PS22A73	107Ω	17.0A
PS22A72	261Ω	8.5A

Condition: Tj=-20°C~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals

Normally, Above Rs values (E96 series) are recommended respectively. If needs to change the trip level, it can be achieved by changing sense resistance. But lower resistance than these values is not permitted.

The SC protection level depends on the sense resistance and the temperature. Their characteristics vs. sense resistance are described from Fig.2-6 to Fig.2-10.

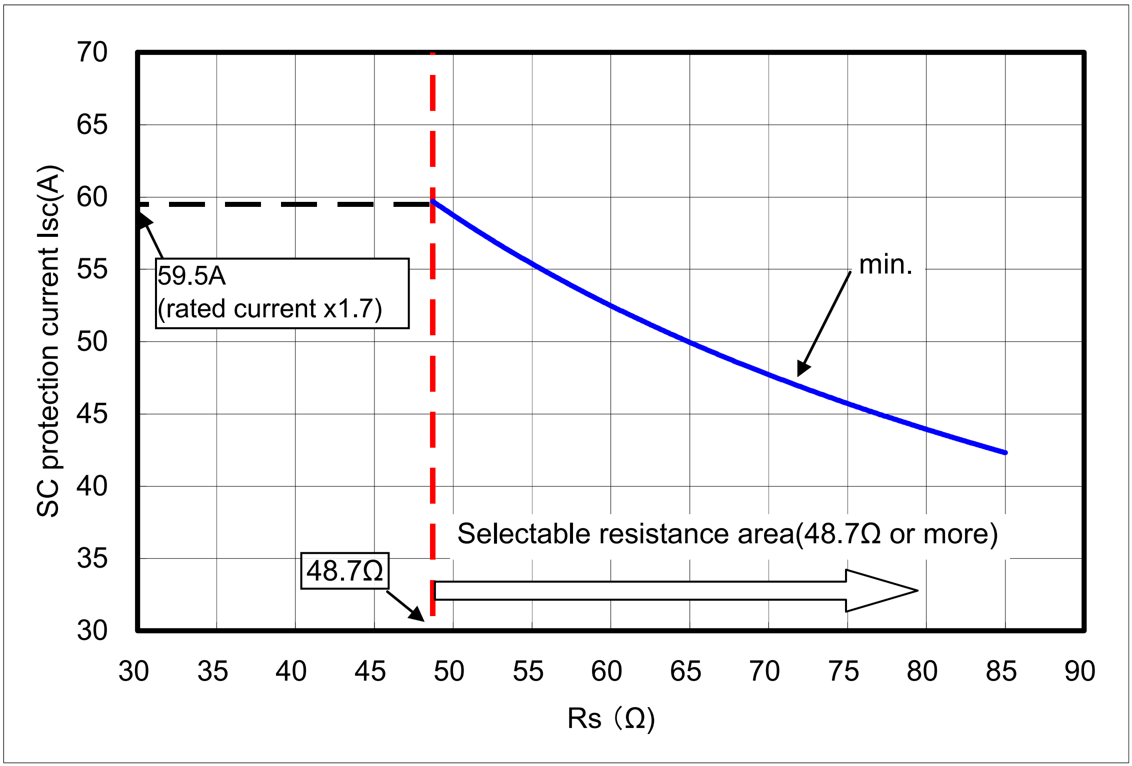


Fig.2-6 Sense resistance Rs vs. SC trip level for PS22A78-E
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)

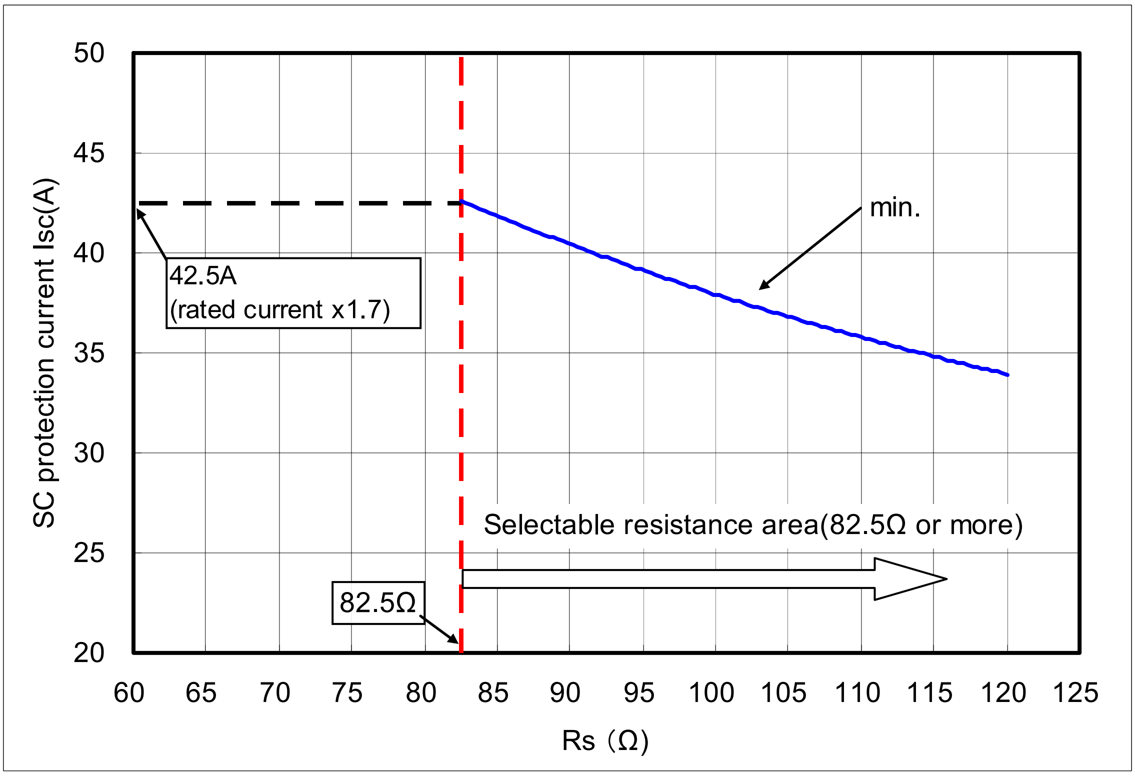


Fig.2-7 Sense resistance Rs vs. SC trip level for PS22A76
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)

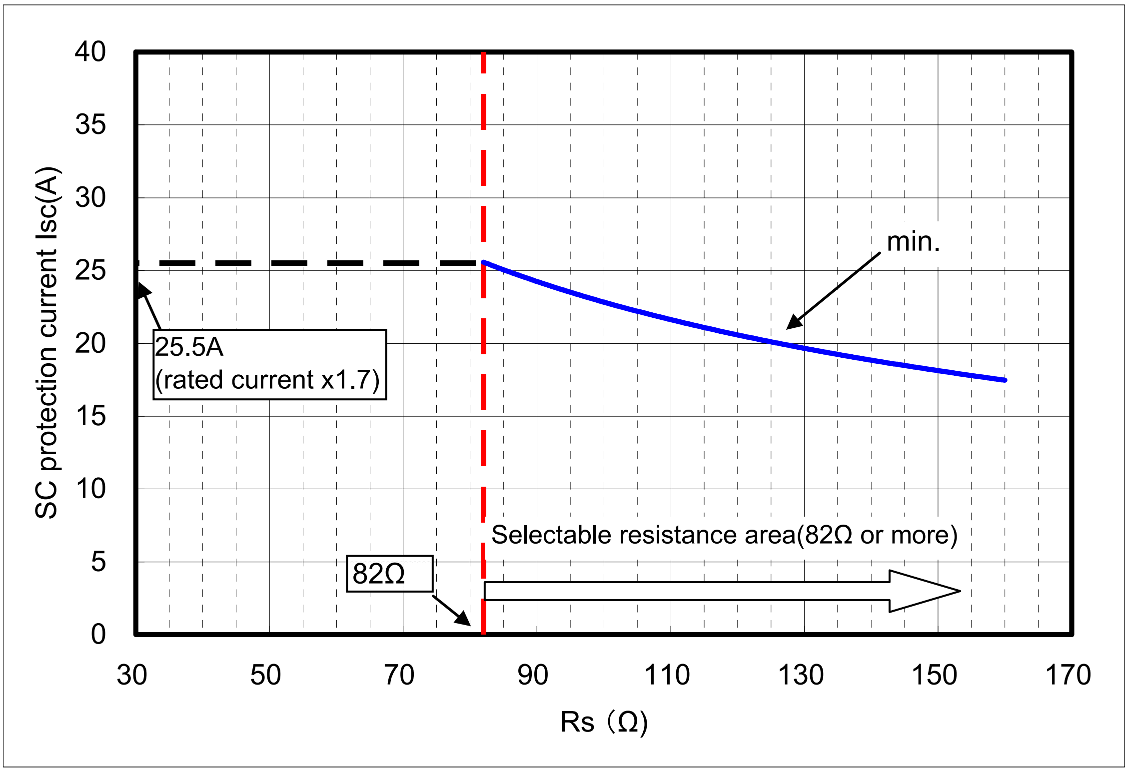


Fig.2-8 Sense resistance Rs vs. SC trip level for PS22A74
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)

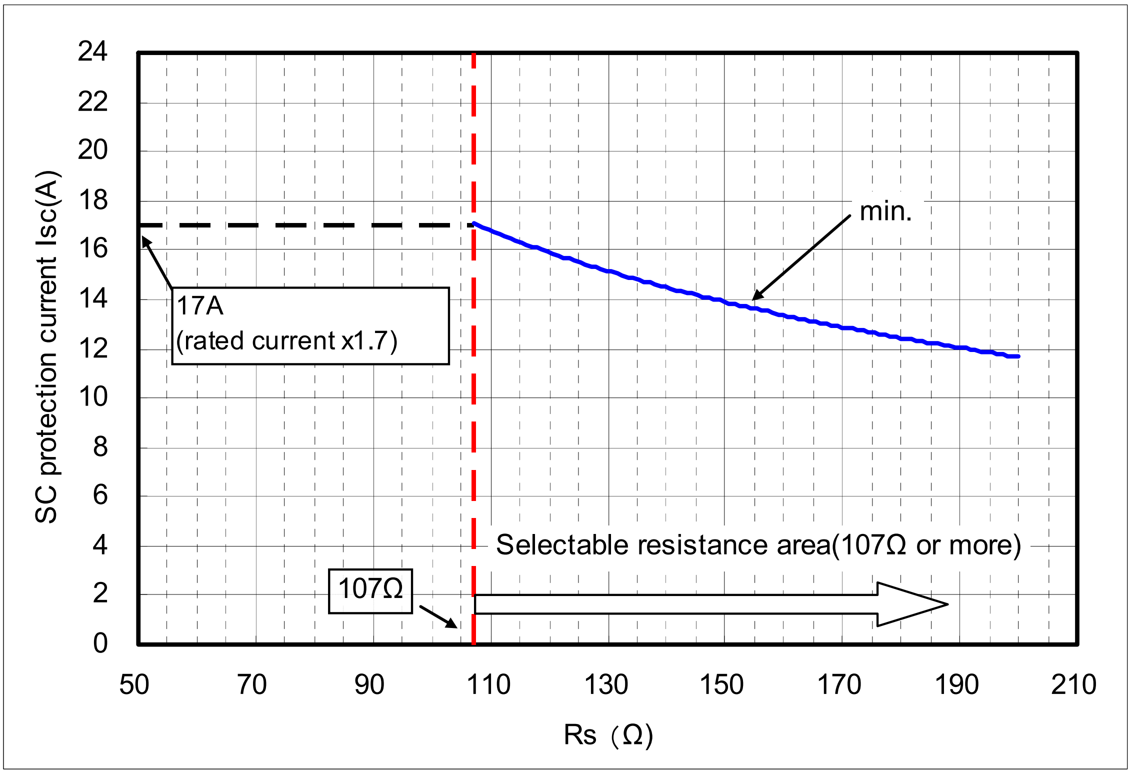


Fig.2-9 Sense resistance Rs vs. SC trip level for PS22A73
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)

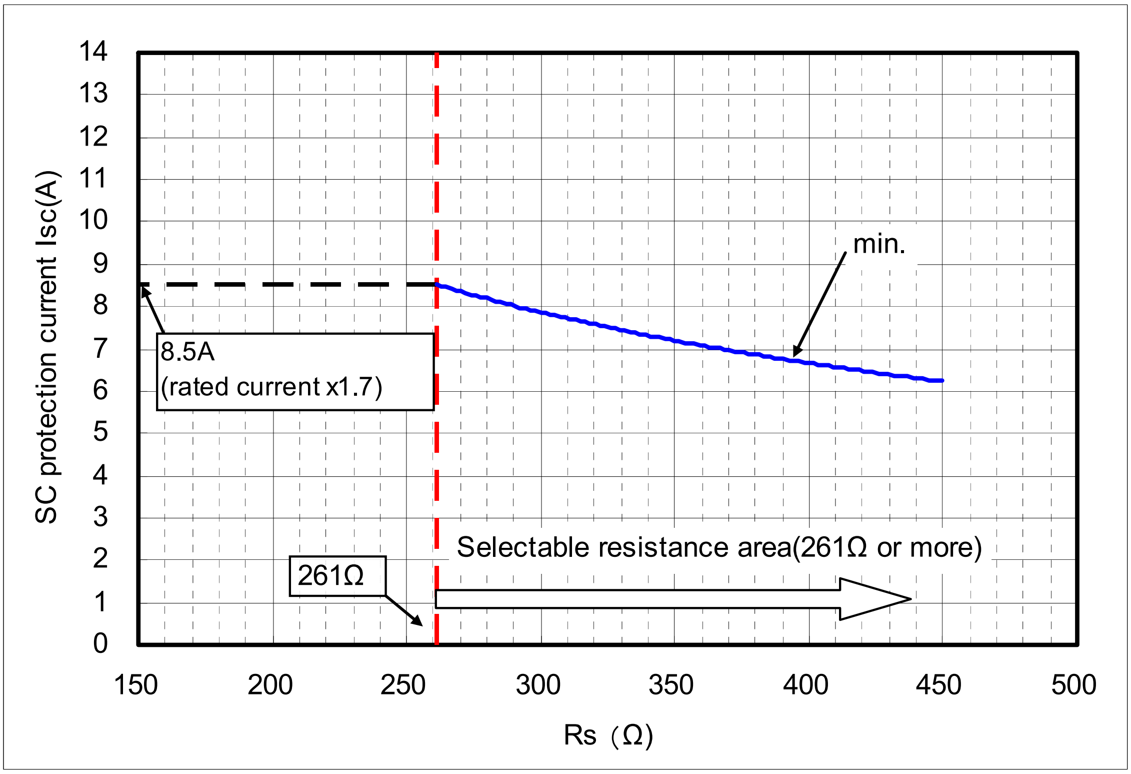


Fig.2-10 Sense resistance Rs vs. SC trip level for PS22A72
(Tj=-20~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals)

For sense resistor, its big fluctuation leads to big fluctuation of SC trip level. So it is necessary to select small variation in the resistance (within +/-1% is recommended).

And its wattage can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 4000:1. (In this case maximum sense current flows.) The estimation example for PS22A78-E is described as below.

[Estimation example]

(1) Normal operation state

It is assumed that the maximum main current for normal operation is 70A (rated current x 2, for keeping a margin) and the sense resistance is 48.7Ω.

In this case, The maximum sense current flows through the sense resistor is calculated as below.

70A / 4000 = 17.5mA

And the loss at the sense resistor is

$P=I^2 \cdot R=(17.5mA)^2 \times 48.7\Omega$ = 15*mW*

(2) Short circuit state

When short circuit occures, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current=350A) flows. So the sense current is

350A / 4000 = 87.5mA

But this current shut down within t=2μs by SC protection. And the average loss at the sense resistor is

$P=I^2 \cdot R \cdot t/T= (87.5mA)^2 \times 48.7\Omega \times 2\mu s / 1s$ =*0.0007mW*

As explained above, over 1/8W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]
It takes more time (like as Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC's transfer delay)

Table 2-8. Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and this IC delay.

SC protection (N-side only, with external resistor and RC filter)
a1. Normal operation: IGBT turn on and carry current.
a2. Short circuit current is detected (SC trigger).
a3. All N-side IGBTs' gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. Fo output with a fixed pulse width (determined by the external capacitance C_{FO}).
a6. Input "L": IGBT off.
a7. Input "H": IGBT on, but during the Fo output period the IGBT will not turn on.
a8. IGBT turns ON when L→H signal is input after Fo is reset.

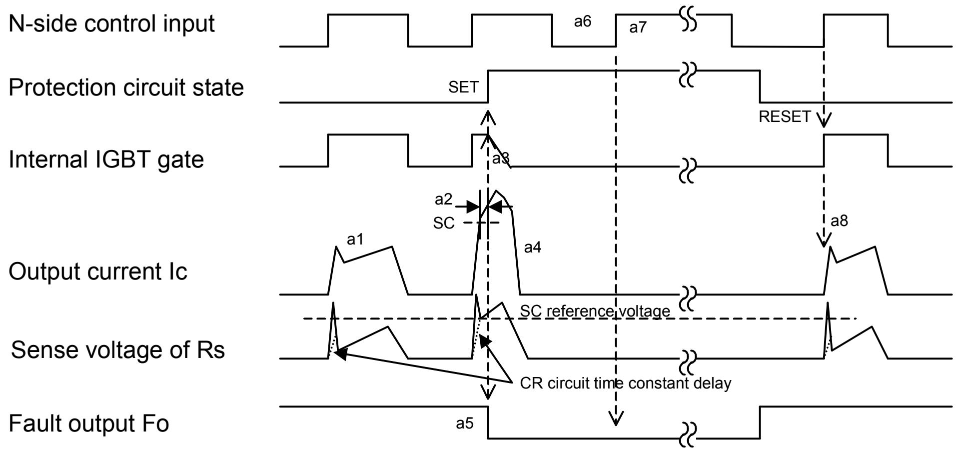


Fig.2-11 SC protection timing chart

2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-9.
Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.
In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-9 DIPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-signals to DIPIPM before the control supply coming up to 13.5V)
4.0-UV trip level (P, N)	UV function become active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV trip level-13.5V(N),13.0V(P)	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions. (Normal operation)
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	Over maximum voltage rating. The control circuit will be destroyed.

<u>Ripple Voltage Limitation of Control Supply</u>

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s, \quad V_{ripple} \leq 2V_{p-p}$$

<u>N-side UV Protection Sequence</u>

a1. Control supply voltage V_D rises: After V_D level reaches under voltage reset level (UV_{Dr}), the circuits start to operate when next input is applied.
a2. Normal operation: IGBT turn on and carry current.
a3. V_D level dips to under voltage trip level. (UV_{Dt}).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo is output for the period determined by the capacitance C_{FO} but continuously during UV period.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: IGBT turn on and carry current.

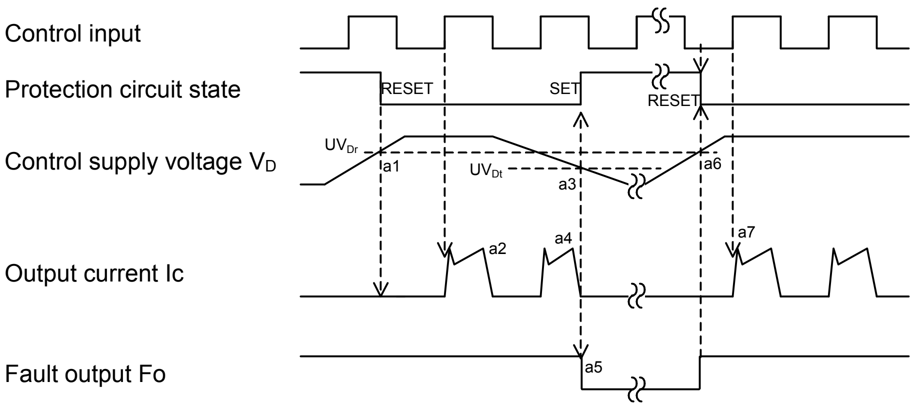


Fig.2-12 Timing chart of N-side UV protection

P-side UV Protection Sequence

b1. Control supply voltage V_{DB} rises : After V_{DB} level reaches under voltage reset level (UV_{DBr}), the circuits start to operate when next input is applied.
b2. Normal operation: IGBT turn on and carry current.
b3. V_{DB} level dips to under voltage trip level (UV_{DBt}).
b4. P-side IGBT turns OFF in spite of control input signal level, but there is no Fo signal output.
b5. V_{DB} level reaches UV_{DBr}.
b6. Normal operation: IGBT turn on and carry current.

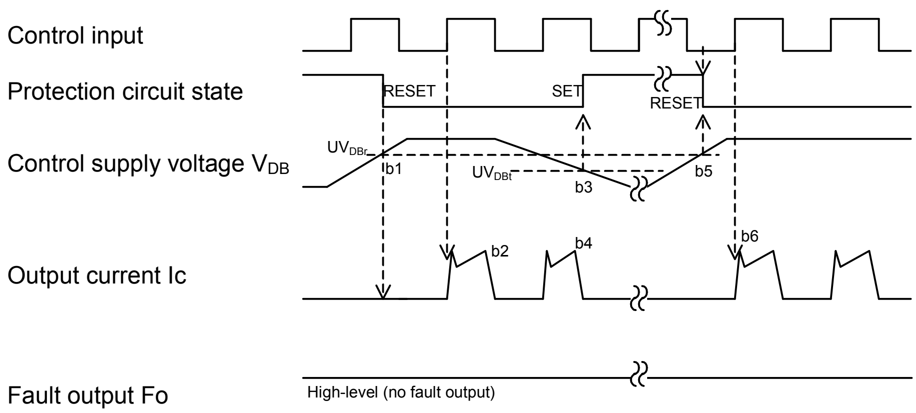


Fig.2-13 Timing Chart of P-side UV protection

2.2.3 Temperature analog output

(1) Purpose of this function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)

It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation.（Replacement from the thermistor which was set on outer heat sink currently）

[Note]

DIPIPM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIPIPM.

(2) V_{OT} characteristics

The characteristics of V_{OT} output vs. LVIC temperature is described as Fig.2-14.

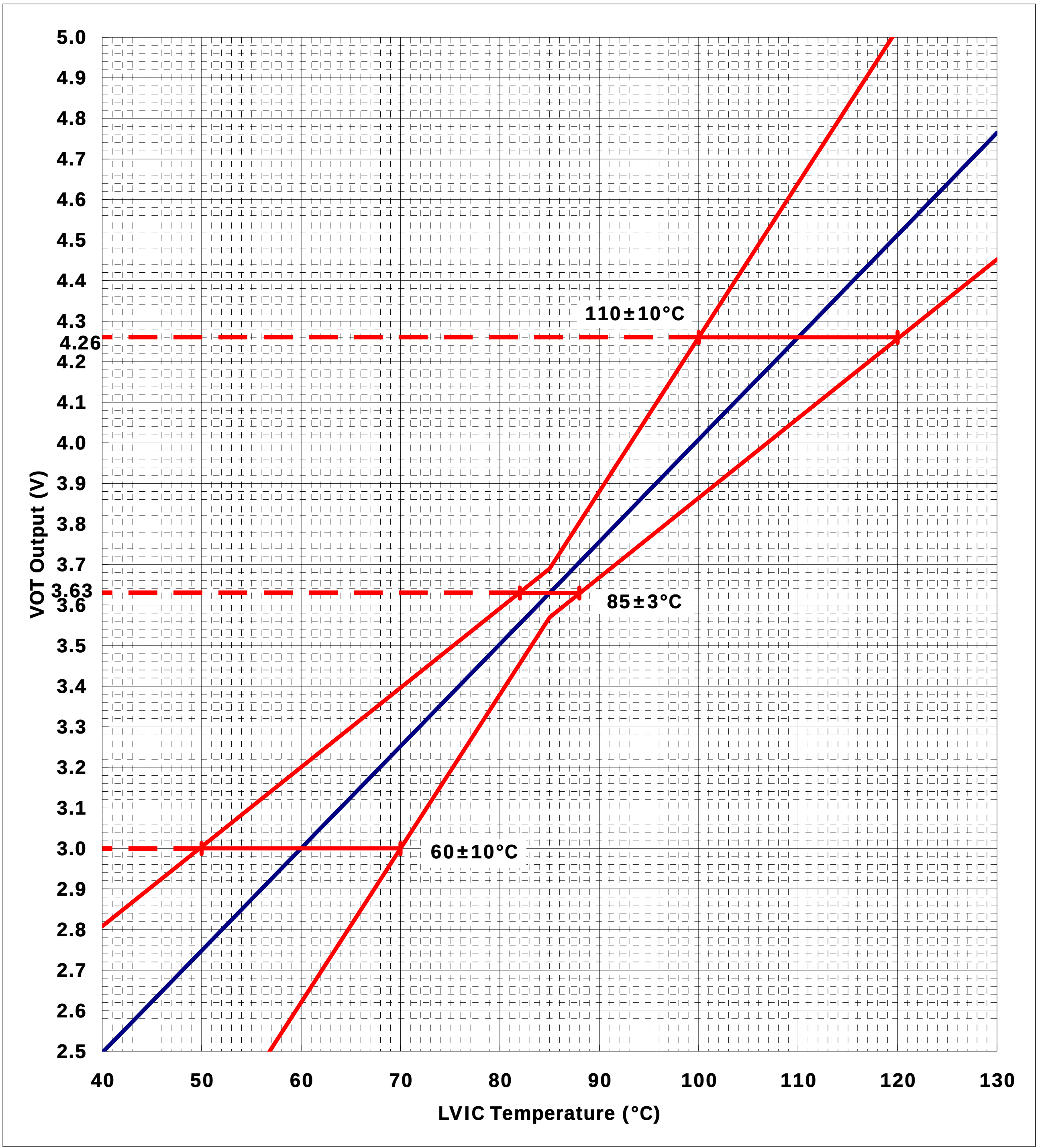


Fig.2-14 V_{OT} output vs. LVIC temperature

As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature: Tic(=V_{OT} output), case temperature: Tc(measuring point is defined on datasheet), and junction temperature: Tj depends on the system cooling condition, heat sink, control strategy, etc.

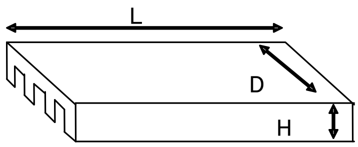
For example, the evaluation results in the case of using different size heat sink (table 2-10) are described as Fig.2-15. As the result of evaluations, it is clear that two cases have different relationships between LVIC temperature Tic and case temperature Tc.

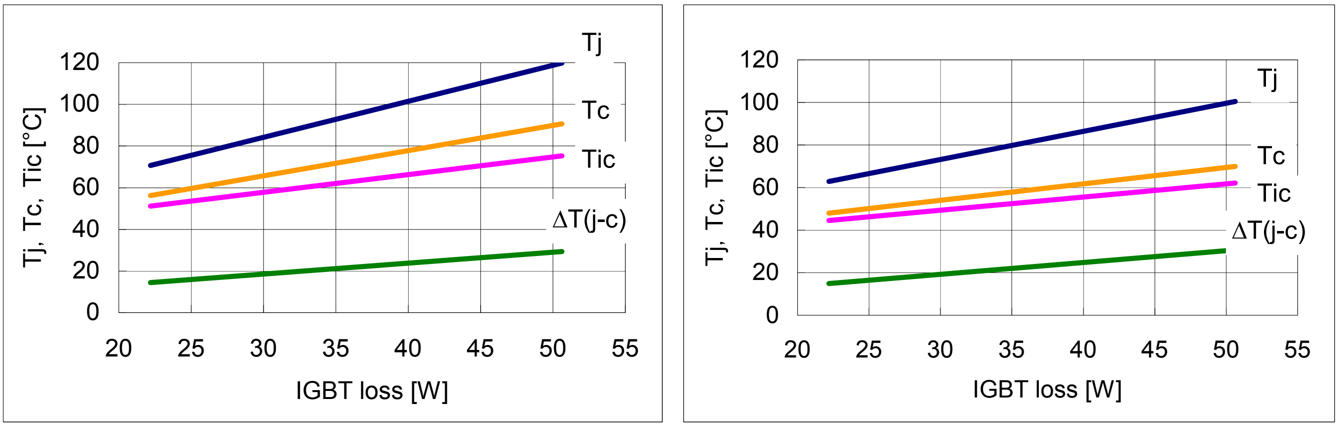
So when setting the threshold temperature for protection, it is necessary to measure the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature is at Tc≤100°C and Tj ≤150°C.

Measuring each temperatures @ only 1 IGBT chip turns on (DC current, Ta=25°C)

Table 2-10 Outer heat sink

	Thermal resistance Rth(f-a)	Heat sink size (L x D x H)
A	2.20K/W	100 x 88 x 40 mm
B	1.35K/W	200 x 88 x 40 mm





(a) Heat sink A (b) Heat sink B

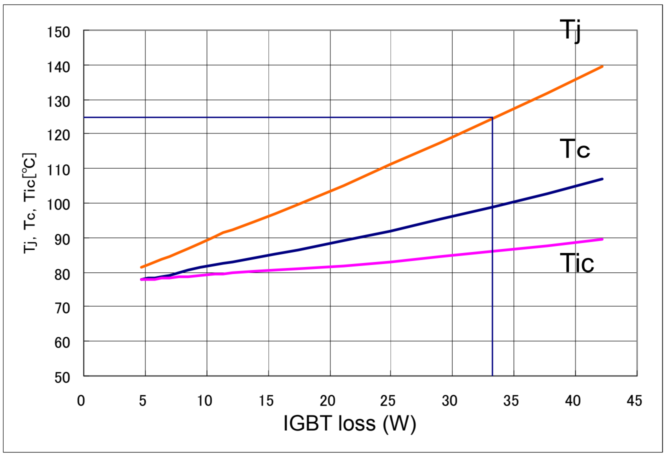
Fig.2-15 IGBT loss vs. Tj, Tc, Tic(Ta=25°C, Typical)

The procedure example of setting protection temperature is described below.

Fig.2-16 indicates the example of the relationship between LVIC temperature Tic, case temperature Tc and junction temperature Tj, and Fig.2-17 is the relationship between V_{OT} and Tc, which is obtained by combining Fig.2-14 and Fig.2-16.

If the protection level is set to Tj=125°C (Tc=100°C), then V_{OT} threshold level should be set 3.75V which is the maximum value @ Tc=100°C in Fig.2-17.

In this case the variation of real Tc may become from 100°C to 115°C. But even if the real Tc will be maximum variation value 115°C, Tj becomes under 150°C (125°C+15°C=140°C<150°C).



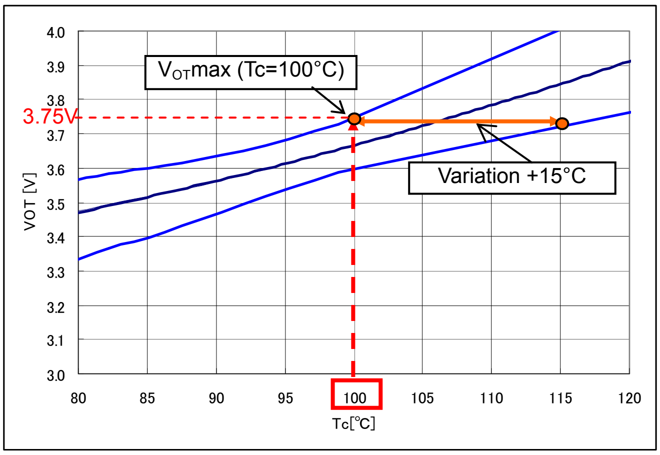


Fig.2-16 IGBT loss vs. Tj, Tc, Tic(Typical) (Ta=80°C) Fig.2-17 V_{OT} vs. Tc (Typical)

As mentioned above, the relationship between Tic, Tc and Tj depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V_{OT} vs. LVIC temperature and the thermocouple for measuring Tj.

(3) Inner circuit of V_{OT} terminal

Inner circuit of V_{OT} terminal is the output of OP amplifier circuit and is described as Fig.2-18

If the resistor is inserted between V_{OT} and V_{NC}(control supply GND) terminals, then the current (calculated by V_{OT} output ÷ resistance of inserted resistor) always flows as circuit current of LVIC.

The current capability of V_{OT} output is described as Table 2-11.

Table 2-11 Output capability (Tc=-20℃~100°C)

	min.
Source	1.7mA
Sink	0.1mA

Source : the current flow from V_{OT} to outside.

Sink : the current flow from outside to V_{OT}.

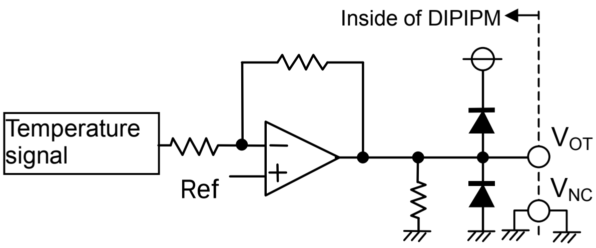


Fig.2-18 Inner circuit of V_{OT} terminal

2.3 Package Outlines

2.3.1 Outline Drawing

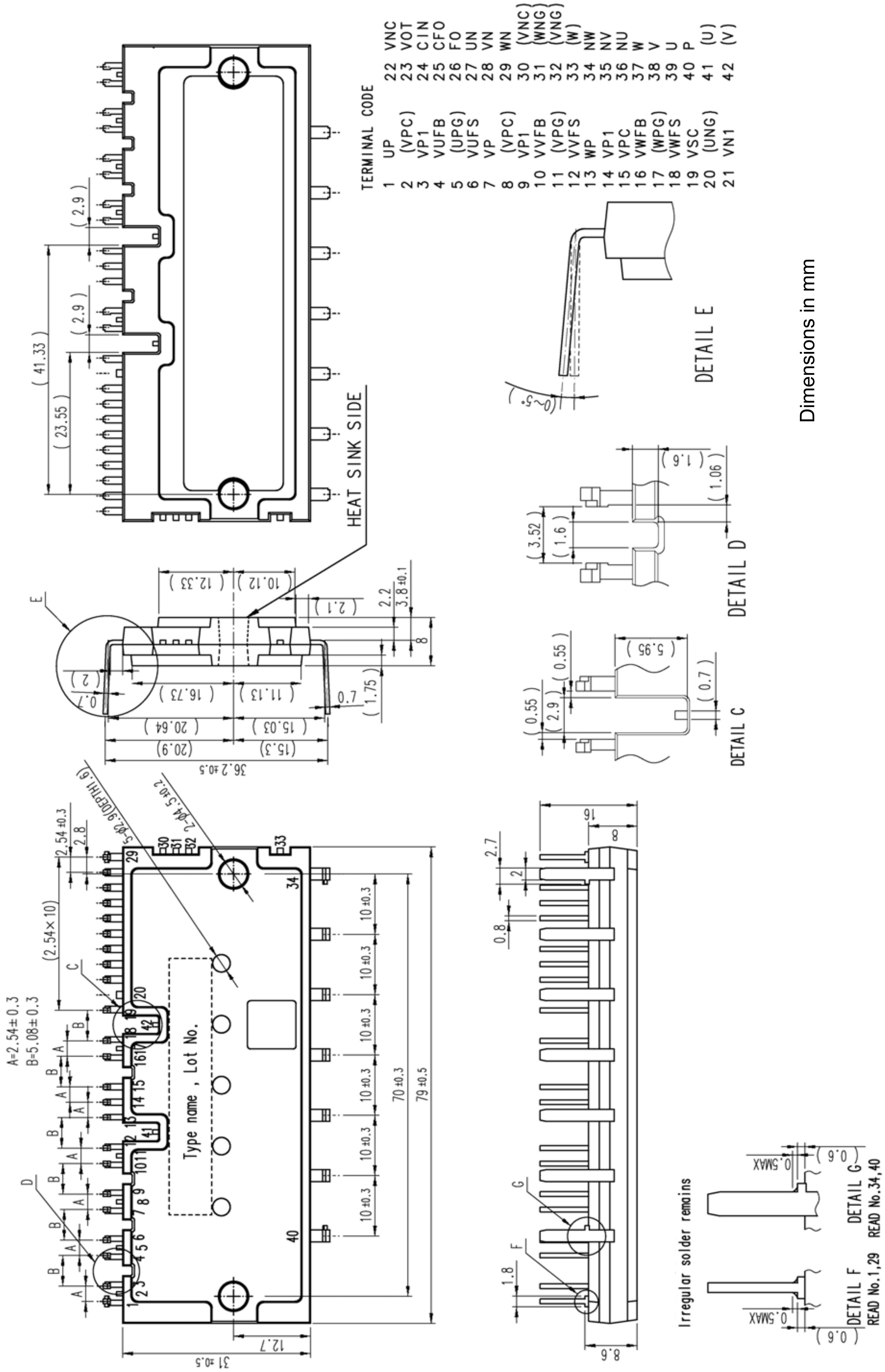


Fig.2-19 Outline drawing

2.3.2 Power Chip Position

Fig.2-20 indicates the center position of the each power chips.
(This figure is the view from laser marked side.)

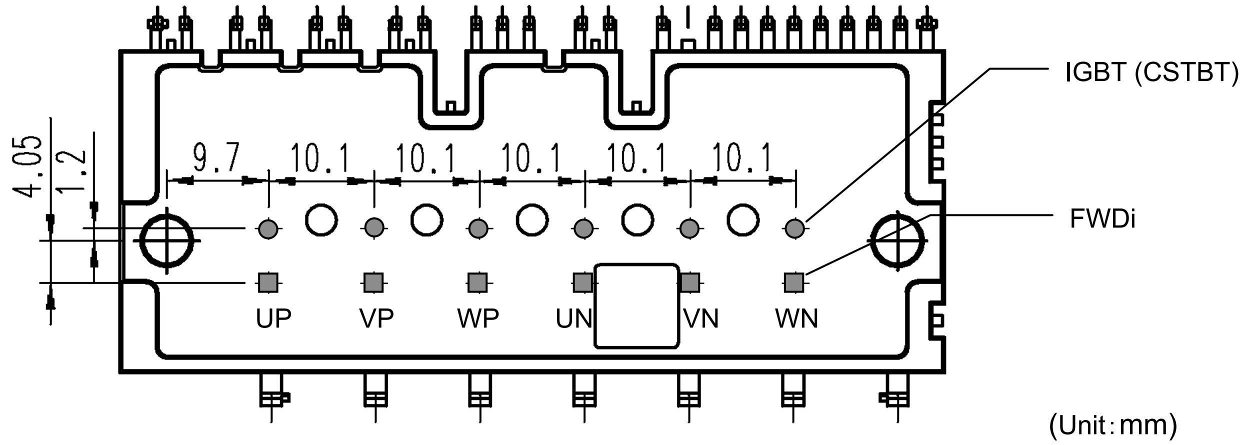
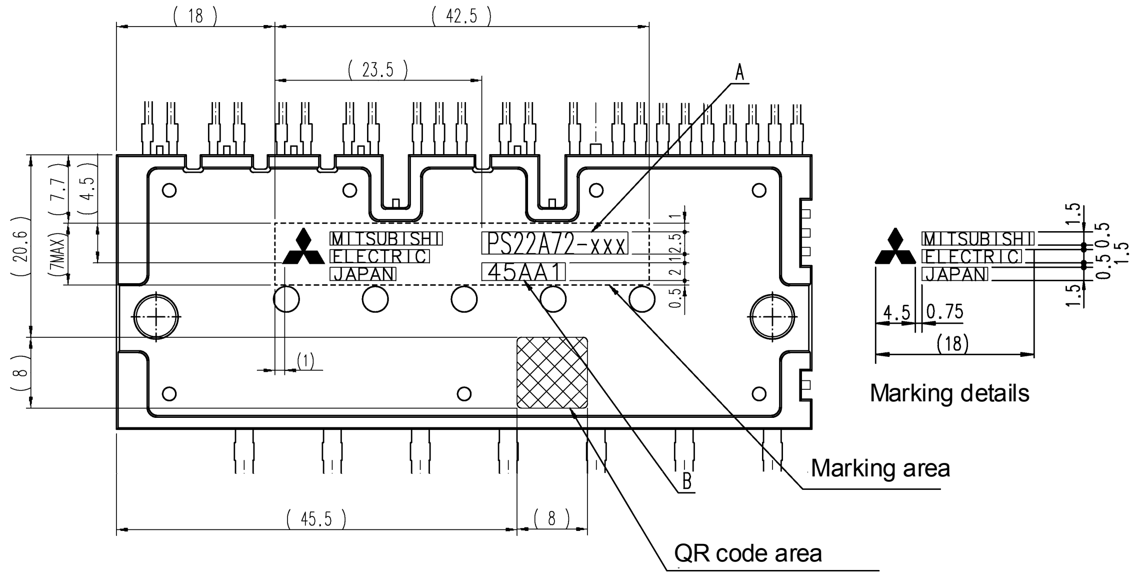


Fig.2-20 Power chip position

2.3.3 Laser Marking Position

The laser marking specification is described in Fig.2-21.
Mitsubishi Corporation mark, Type name (A), Lot number (B), and QR code mark are marked in the upper side of module.



QR Code is registered trademark of DENSO WAVE INCORPORATED in JAPAN and other countries.

Fig.2-21 Laser marking view

2.3.4 Terminal Description

Table 2-12 Terminal description

No.	Name	Description
1	U_P	U-phase P-side control input terminal
3	V_{P1}	U-phase P-side control supply positive terminal
4	V_{UFB}	U-phase P-side drive supply positive terminal
6	V_{UFS}	U-phase P-side drive supply GND terminal
7	V_P	V-phase P-side control input terminal
9	V_{P1}	V-phase P-side control supply positive terminal
10	V_{VFB}	V-phase P-side drive supply positive terminal
12	V_{VFS}	V-phase P-side drive supply GND terminal
13	W_P	W-phase P-side control input terminal
14	V_{P1}	W-phase P-side control supply positive terminal
15	V_{PC}	P-side control supply GND terminal
16	V_{WFB}	W-phase P-side drive supply positive terminal
18	V_{WFS}	W-phase P-side drive supply GND terminal
19	V_{SC}	Sense current detecting terminal
21	V_{N1}	N-side control supply positive terminal
22	V_{NC}	N-side control supply GND terminal
23	V_{OT}	LVIC temperature output terminal
24	CIN	SC trip voltage detect terminal
25	CFO	Fault pulse output width set terminal
26	F_O	Fault signal output terminal
27	U_N	U-phase N-side control input terminal
28	V_N	V-phase N-side control input terminal
29	W_N	W-phase N-side control input terminal
34	NW	W-phase N-side IGBT emitter terminal
35	NV	V-phase N-side IGBT emitter terminal
36	NU	U-phase N-side IGBT emitter terminal
37	W	W-phase output terminal
38	V	V-phase output terminal
39	U	U-phase output terminal
40	P	Inverter DC-link positive terminal

No.	Name	Description
2	V_{PC}	Internal use (Dummy pin) Don’t connect all dummy pins to any other terminals or PCB pattern. (Leave no connect)
5	U_{PG}	
8	V_{PC}	
11	V_{PG}	
17	W_{PG}	
20	U_{NG}	
30	V_{NC}	
31	W_{NG}	
32	V_{NG}	
33	W	
41	U	
42	V	

Table 2-13 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIPIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{PC} V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. Voltage input type. • These terminals are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Because more noisy in the application for 1200V, it is strongly recommended to insert RC filter. (time constant: over 100ns. e.g. 100Ω, 1000pF) • In the case of using RC filter, pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Sense current detect terminal	V_{SC}	• The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.
Short-circuit trip voltage detecting terminal	CIN	• Input the potential of Vsc terminal (with sense resisteor) to CIN terminal for SC protection through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal for N-side abnormal state(SC or UV). • This output is open drain type. F_O signal line should be pulled up to a 5V logic supply with over 5kΩ resistor (for limitting the Fo sink current I_{Fo}up to 1mA.) Normally 10kΩ is recommended.
Fault pulse output width setting terminal	CFO	• The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and VNC. • When 22nF capacitor is connected, then the Fo pulse width becomes 2.4ms. $t_{FO} = C_{FO} / (9.1 \times 10^{-6})$ (s)
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU,NV,NW	• Open emitter terminal of each N-side IGBT • If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions.

2.4.1 Electric Spacing

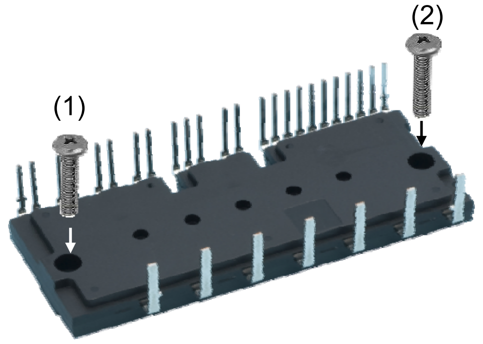
The electric spacing specification of Large DIPIPM Ver.4 is shown in Table 2-14

Table 2-14 Minimum insulation distance

	Clearance (mm)	Creepage (mm)
Between live power terminals with high potential	7.1	7.9
Between live control terminals with high potential	3.3	5.6
Between terminals and heat sink	3.7	5.6

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the device. The recommended fastening procedure is shown in Fig.2-22. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-22 Recommended screw fastening order

Table 2-15. Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 1.18N·m, Screw : M4	0.98	-	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-23	-50	-	+100	μm

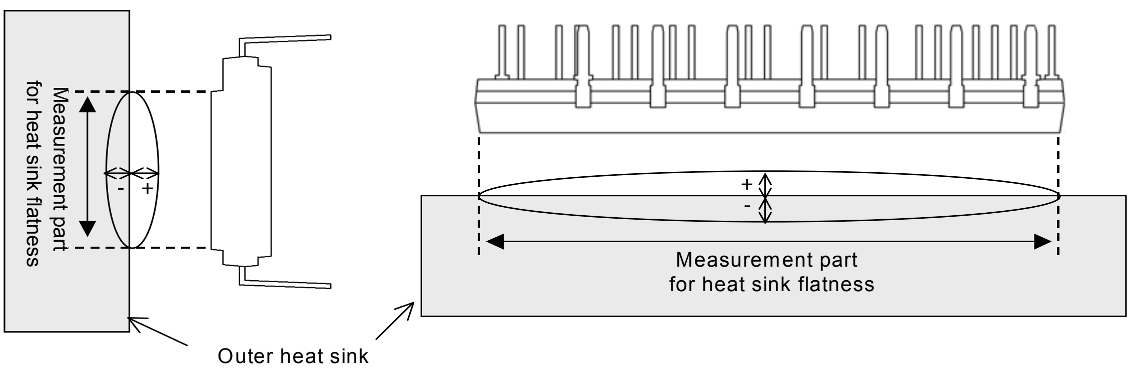


Fig.2-23 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2°C/W (per 1/6 module, grease thickness: 20μm ,thermal conductivity: 1.0W/m·k).

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in table 2-16 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-16 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample : Large DIPIPM Ver.4

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

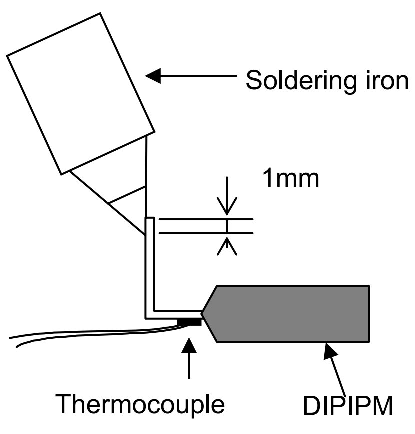


Fig.2-24 Heating and measuring point

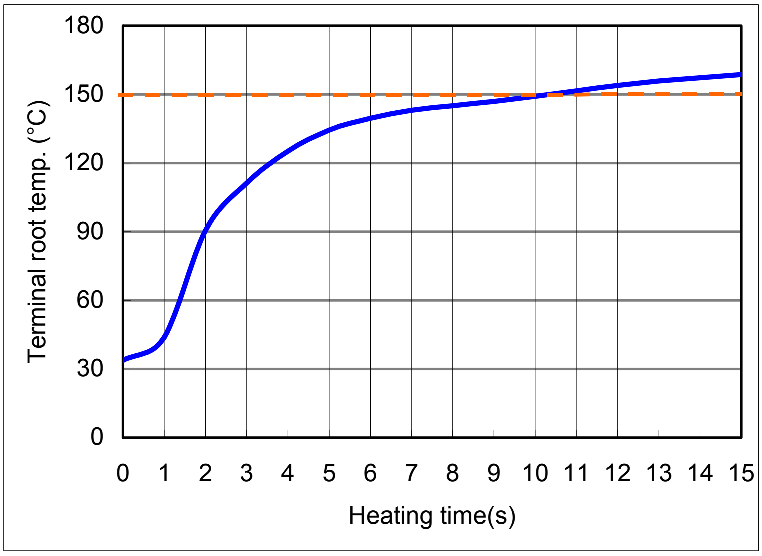


Fig.2-25 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance

This chapter states usage and interface circuit design hints.

3.1.1 System connection

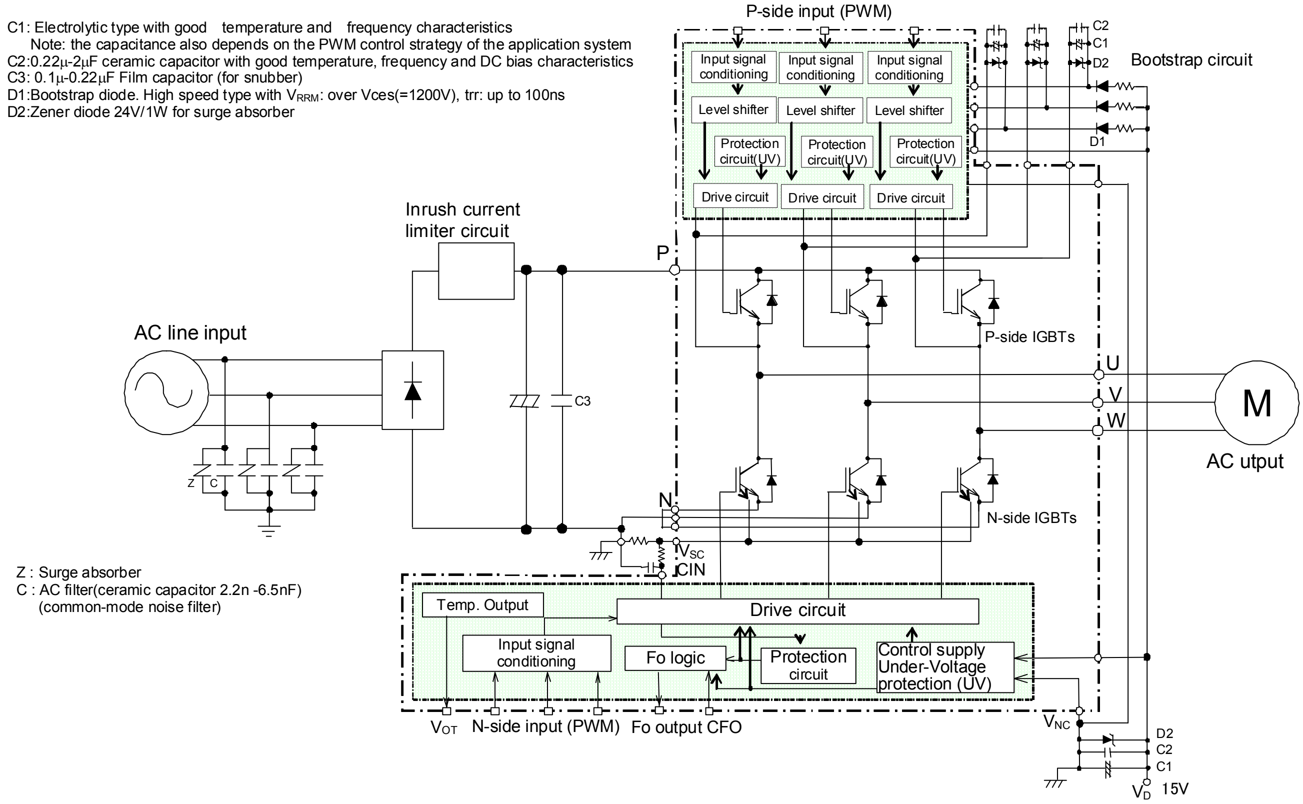


Fig.3-1 Application System block diagram

3.1.2 Interface Circuit (Direct Coupling Interface example)

Fig.3-2 shows a typical application circuit of interface schematic, in which control signals are transfered directly from a controller (MCU or DSP).

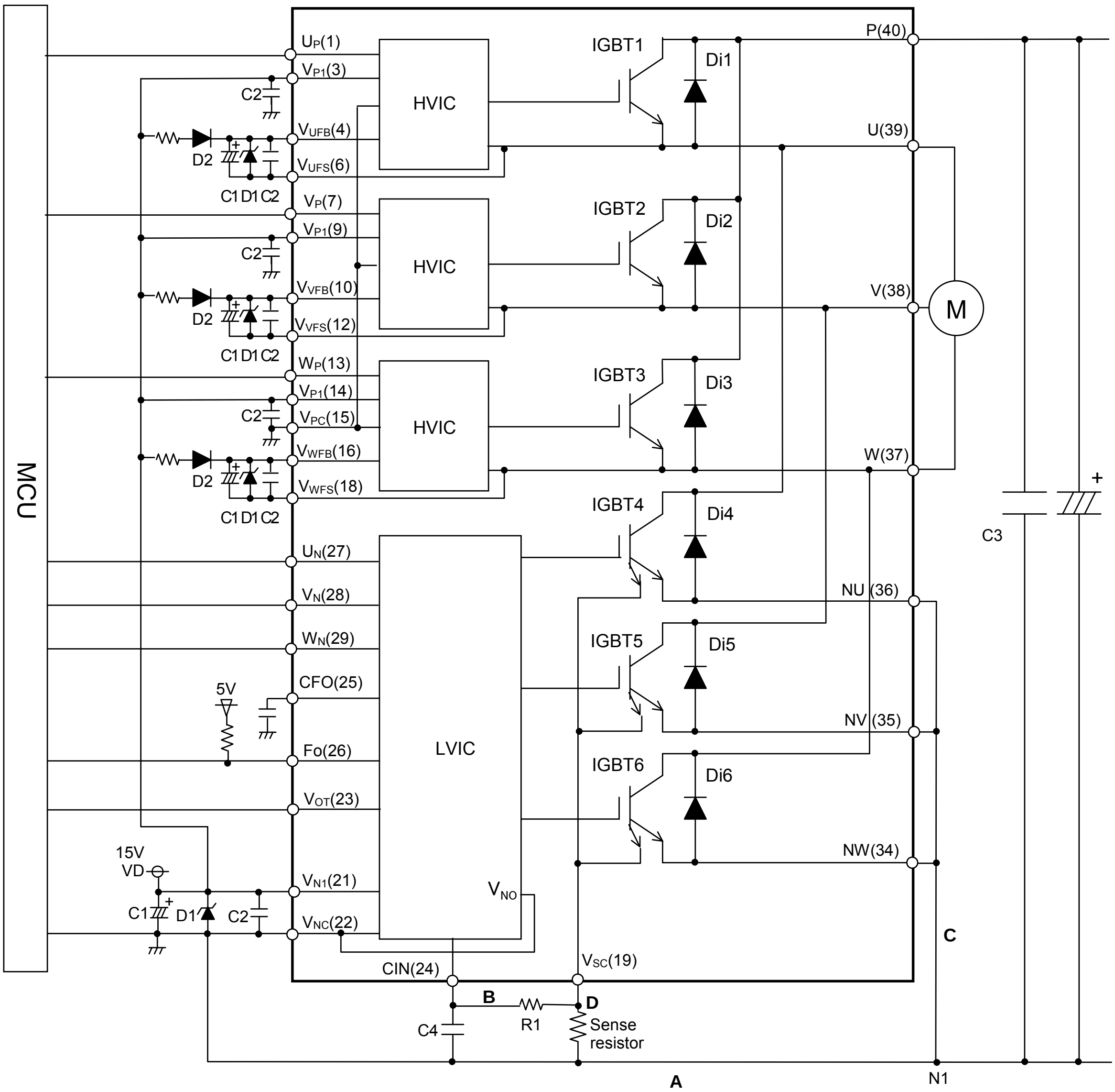


Fig.3-2 Interface circuit example (Direct coupling)

Note:

(1) If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

(2) To prevent surge destruction, the wiring between the smoothing capacitor and the P,N1 terminals should be as short as possible. Generally inserting a 0.1μ~0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

(3) The time constant R1C4 of RC filter for preventing the protection circuit malfunction should be selected in the range of 1.5μs~2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C4

(4) All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(5) It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.

(6) To prevent erroneous SC protection, the wiring from V_{SC} terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.

(7) For sense resistor, the variation within 1% (including temperature characteristics), low inductance type is recommended. And the over 1/8W is recommended, but it is necessary to evaluate in your real system finally.

(8) To prevent erroneous operation, the wiring of A, B, C should be as short as possible.

(9) Fo output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits Fo sink current I_{Fo} under 1mA. In the case pull up to 5V supply, over R2=5.1kΩ is needed. (10kΩ is recommended.)

(10) Error signal output width (t_{Fo}) can be set by the capacitor connected to CFO terminal. t_{Fo}(typ.) $=C_{FO}/(9.1\times10^{-6})$(s)

(11) High voltage (V_{RRM} =1200V or more) and fast recovery type (trr=less than 100ns or less) diode D2 should be used in the bootstrap circuit.

(12) Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be patterned as short as possible. And it is strongly recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

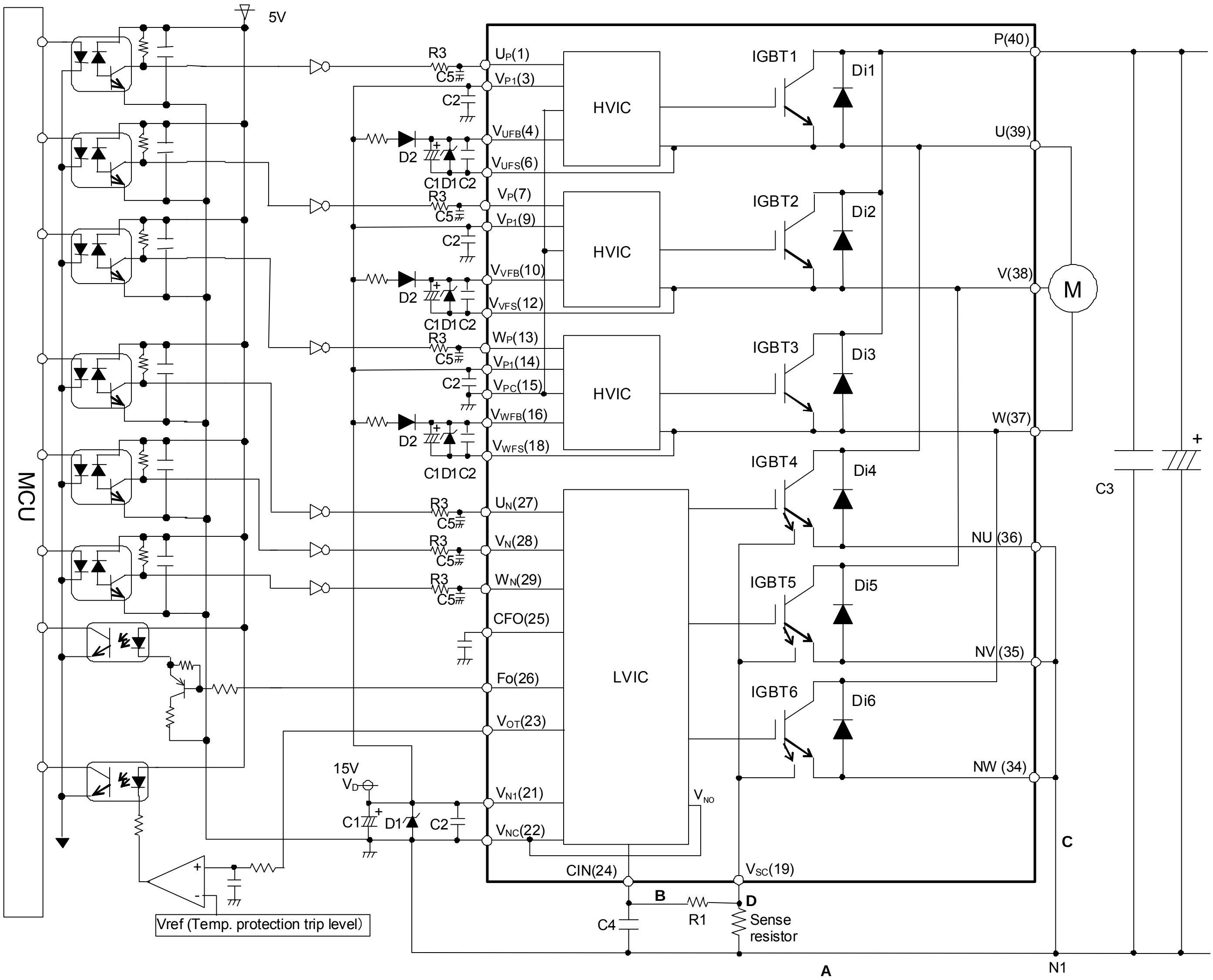


Fig.3-3 Interface circuit example with opto-coupler

Note:

(1) High speed (high CMR) opto-coupler is recommended.
(2) Fo terminal sink current is max.1mA. A buffer circuit is necessary to drive an opto-coupler.
(3) To prevent malfunction, it is strongly recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) close to the terminals and confirm the input signal level to meet the turn-on and turn-off threshold voltage.

3.1.4 Circuits of Signal Input terminals and Fo Terminal

Large DIPIPM Ver.4 is high-active input logic. A 3.3kΩ(min) pull-down resistor is built-in each input circuit of the DIPIPM as shown in Fig.3-4, so external pull-down resistor is not needed.

If the same pattern PCB is used for 600V Large DIPIPM Ver.4 and 1200V Large DIPIPM Ver.4, pay attention to the input threshold voltage. (Their threshold voltages are different.)

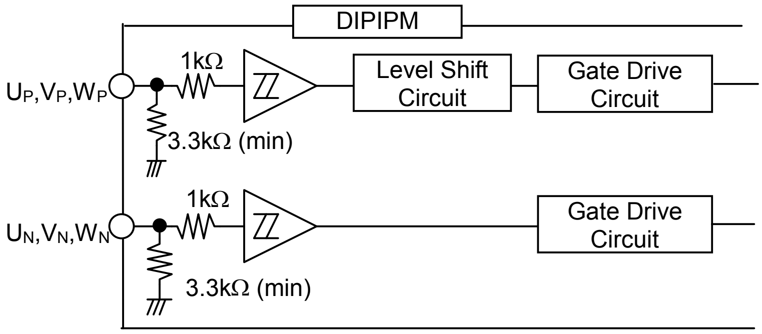


Fig.3-4 Internal structure of control input terminals

Table 3-1 Input threshold voltage ratings (VD=15V, Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{PC} U_N,V_N,W_N-V_{NC}	-	-	3.5	V
Turn-off threshold voltage	Vth(off)		0.8	-	-	

The wiring of each input should be patterned as short as possible. And more noisy in the application for 1200V, so it is strongly recommended to insert RC filter.

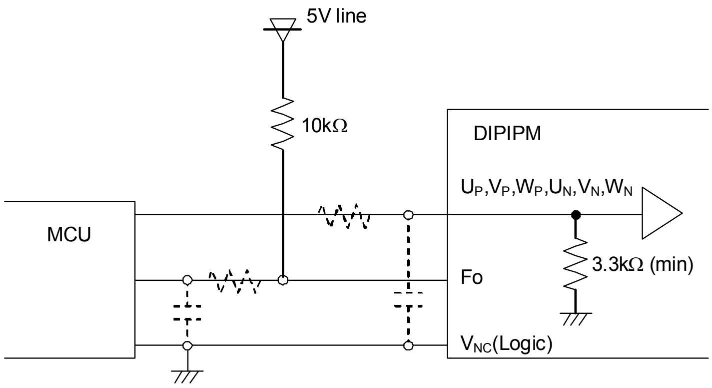


Fig.3-5 Control input connection

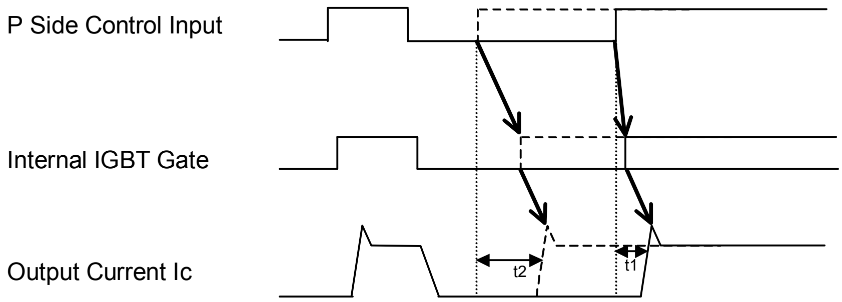
Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

There are limits for the minimum input pulse width in the DIPIPM. The DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Please refer Table 3-2)

Table 3-2 Allowable minimum input pulse width

	Symbol	Condition		PN	Min. value	Unit
On signal	PWIN(on)	-		PS22A72	2.0	μs
				PS22A73	2.0	
				PS22A74	2.0	
				PS22A76	1.5	
				PS22A78-E	1.5	
Off signal	PWIN(off)	$200 \leq V_{CC} \leq 350V$, $13.5 \leq V_D \leq 16.5V$, $13.5 \leq V_{DB} \leq 18.5V$, $-20 \leq T_C \leq 100°C$, N line wiring inductance less than 10nH	Up to rated current	PS22A72	2.5	
				PS22A73	2.5	
				PS22A74	2.5	
				PS22A76	2.3	
				PS22A78-E	2.3	
			From rated current to 1.7x rated current	PS22A72	2.9	
				PS22A73	2.9	
				PS22A74	2.9	
				PS22A76	2.9	
				PS22A78-E	2.9	

*) Input signal with ON pulse width less than PWIN(on) might make no response.
IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).
Please refer Fig.3-6 about delayed response .



Real line···off pulse width>PWIN(off); turn on time t1
Broken line···off pulse width<PWIN(off); turn on time t2

Fig.3-6 Delayed Response with shorter input off (P-side only)

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to control supply (e.g. 5V) as shown in Fig.3-5.
Fig.3-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA.
(I_{Fo} can be estimated from I_{Fo}=*control supply voltage / pull up resistance* approximately.)
If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-3 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V,Fo=10kΩ, 5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V,Fo=1mA	-	-	0.95	V

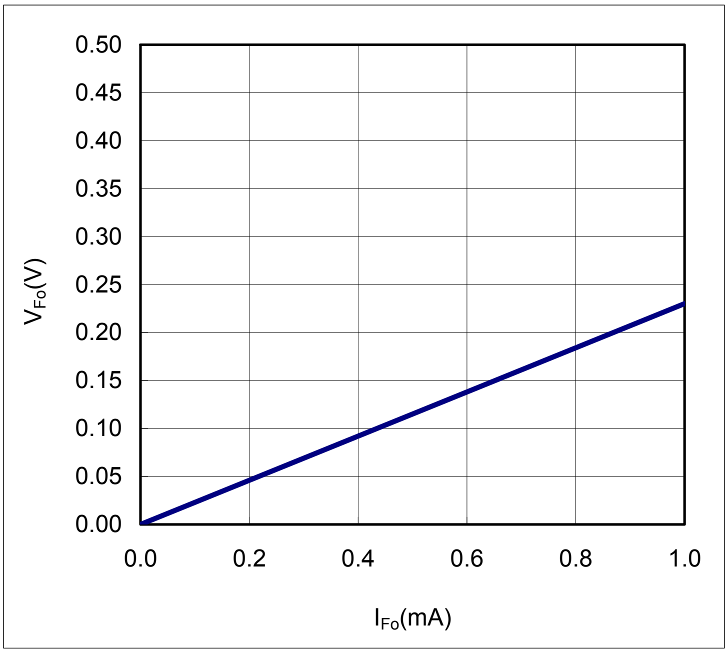


Fig.3-7 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.5 Snubber Circuit

In order to prevent DIPIPM from the surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.
(Its withstand voltage should be over Vces(=power chip's withstand voltage).)

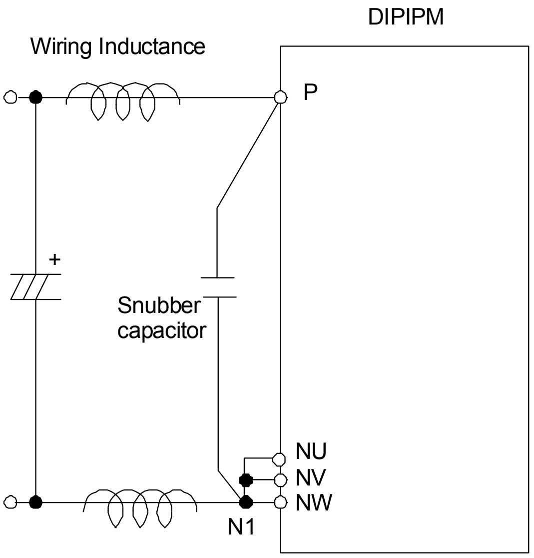


Fig.3-8 Recommended snubber circuit position

3.1.6 Influence of wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

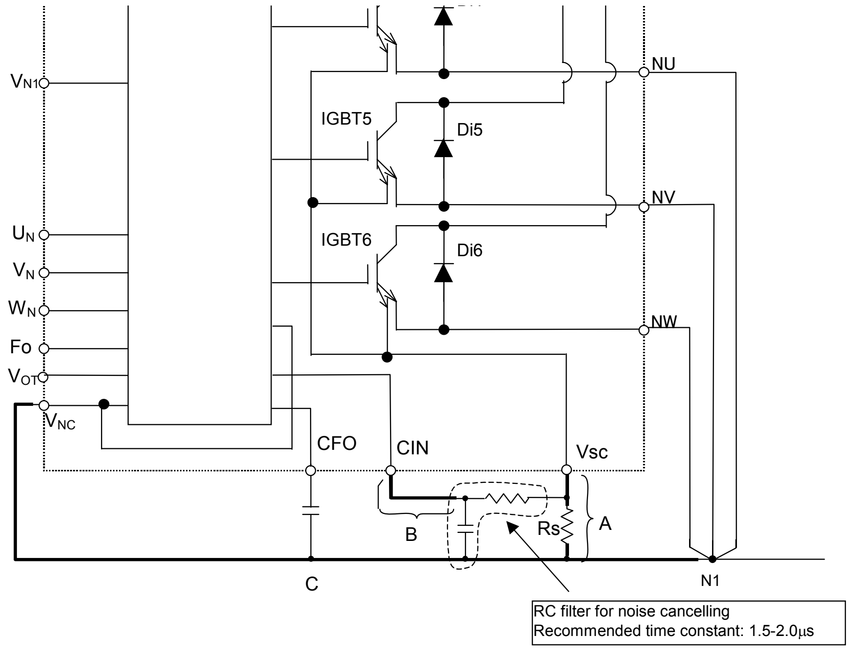


Fig.3-9 External protection circuit

(1) Influence of the part-A wiring

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) Influence of the part-B wiring pattern

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will dropdown and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, VNC terminals as close as possible.

(3) Influence of the part-D wiring pattern

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

3.1.7 Precaution for wiring on PCB

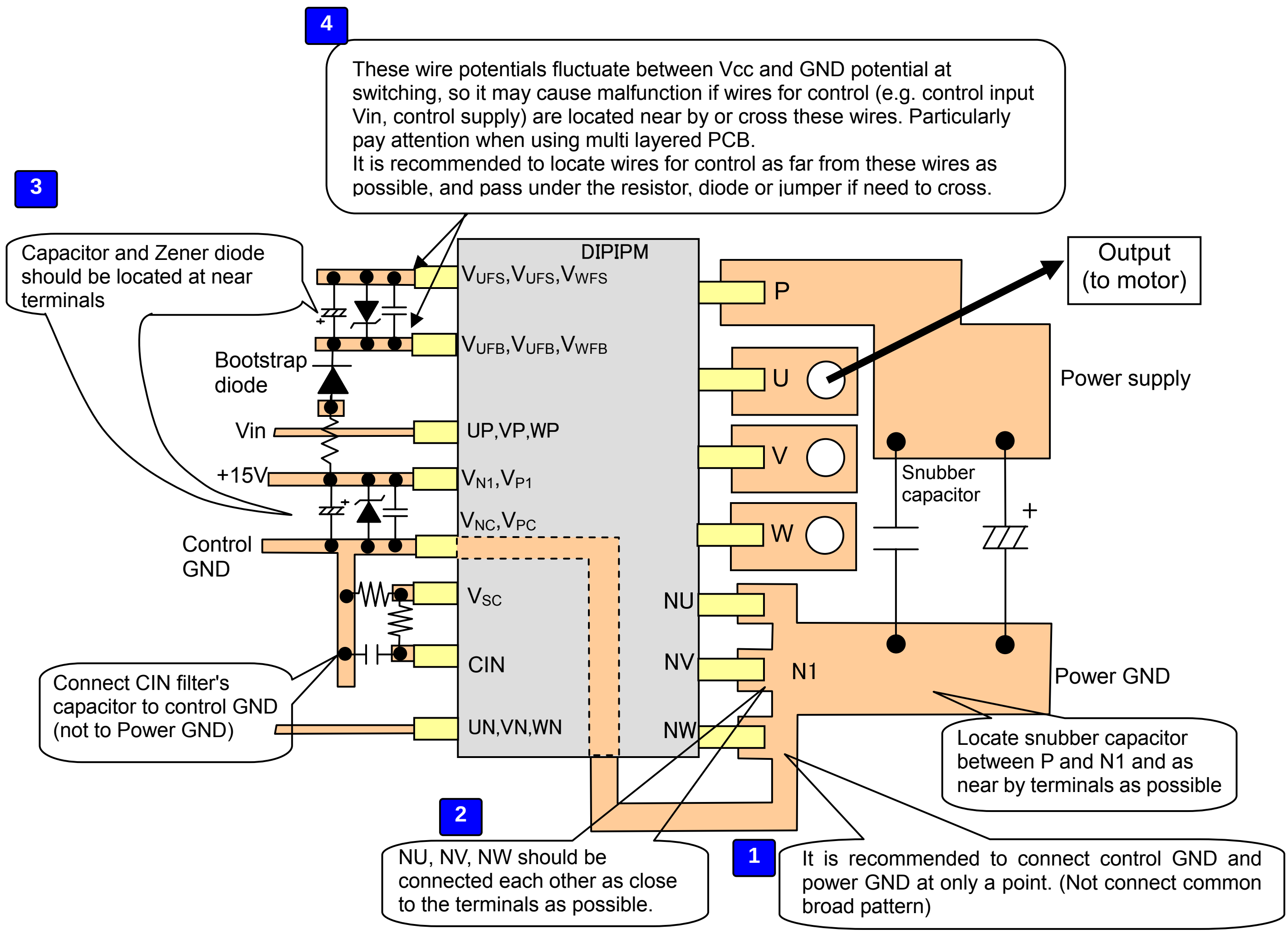


Fig.3-10 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. it causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.
	•Ground loop pattern is existing.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs.
2	•Long pattern between NU, NV, NW terminals and N1	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction by VS voltage (output terminal potential) decreasing excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	The cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then since the incorrect signals are input to DIPIPM, the arm short circuit might occur.

3.1.8 SOA of DIPIPM

The following describes the SOA (Safety Operating Area) of DIPIPM.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: The total amount of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(PROT)}$: DC-link voltage that DIPIPM can protect itself.

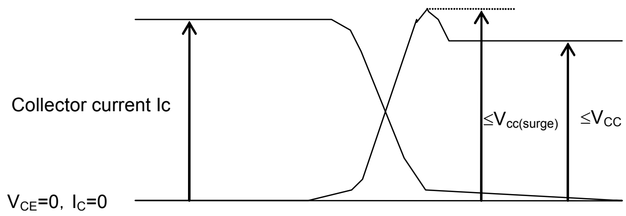


Fig.3-11 SOA at switching mode

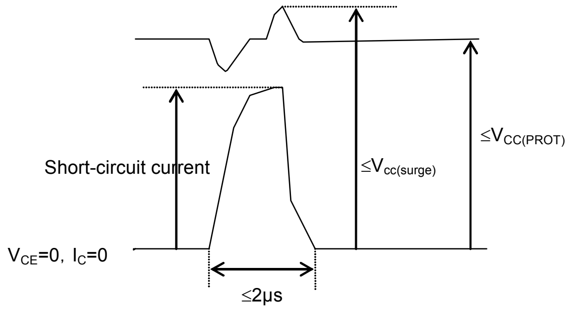


Fig.3-12 SOA at short-circuit mode

<u>In Case of switching</u>

V_{CES} represents the maximum voltage rating (1200V) of the IGBT. By subtracting the surge voltage (200V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 1000V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC}, that is 900V.

<u>In Case of Short-circuit</u>

V_{CES} represents the maximum voltage rating (1200V) of the IGBT . By Subtracting the surge voltage (200V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 1000V. Furthermore, by subtracting the surge voltage (200V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC}, that is, 800V.

3.1.9 SCSOA

Fig.3-13 to Fig.3-17 show the typical SCSOA performance curves of 1200V Large DIPIPM Ver.4 series.
Conditions: Vcc=800V, Tj=125°C at initial state, Vcc(surge)≤1000V(surge included), non-repetitive, 2m load.

The DIPIPM can shutdown safely the SC current that is about 7 to 10 times of its current rating under the conditions only if the IGBT conducting period is less than about 7.0μsec.
Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and so on, it is necessary to set time constant of RC filter with a margin.

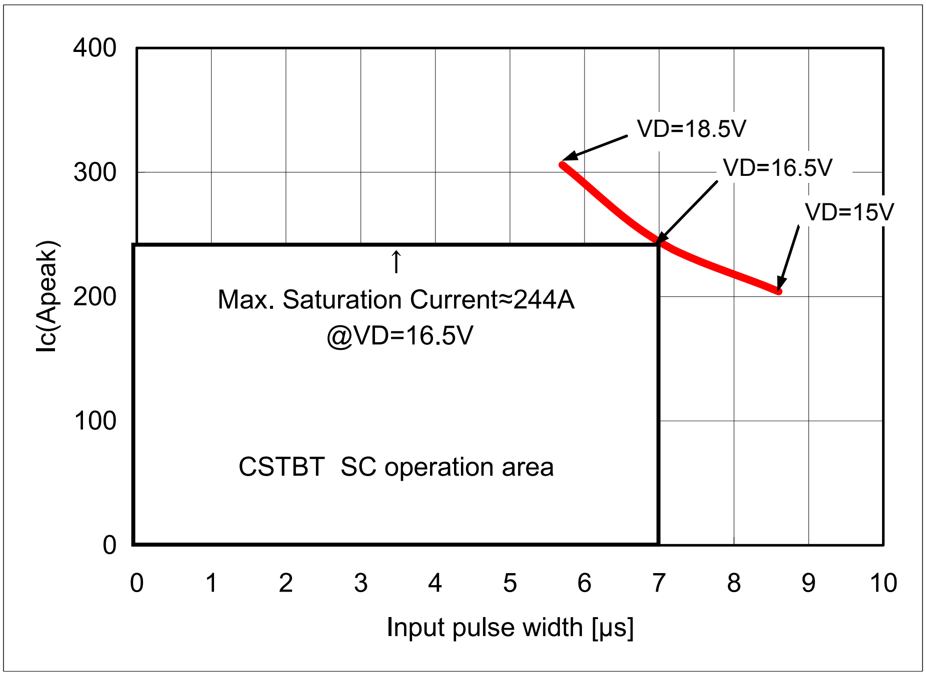


Fig.3-13 PS22A78-E typical SCSOA curve

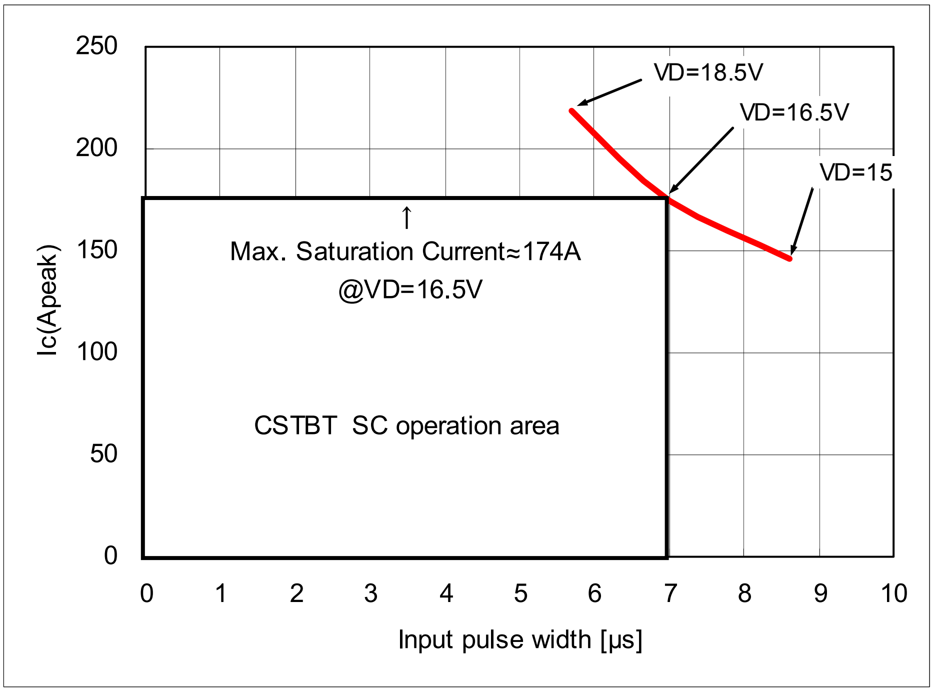


Fig.3-14 PS22A76 typical SCSOA curve

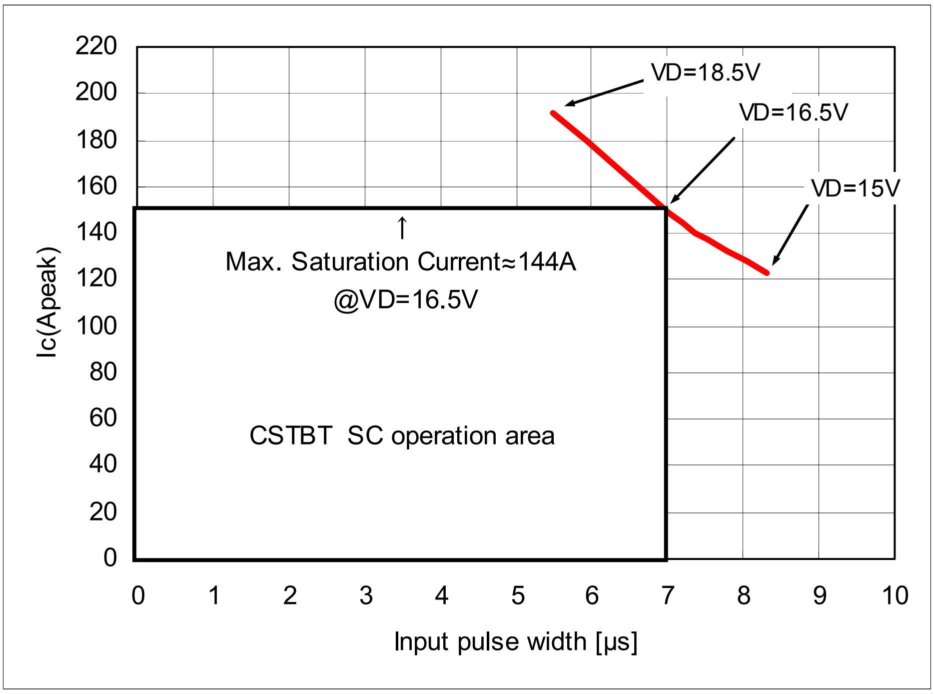


Fig.3-15 PS22A74 typical SCSOA curve

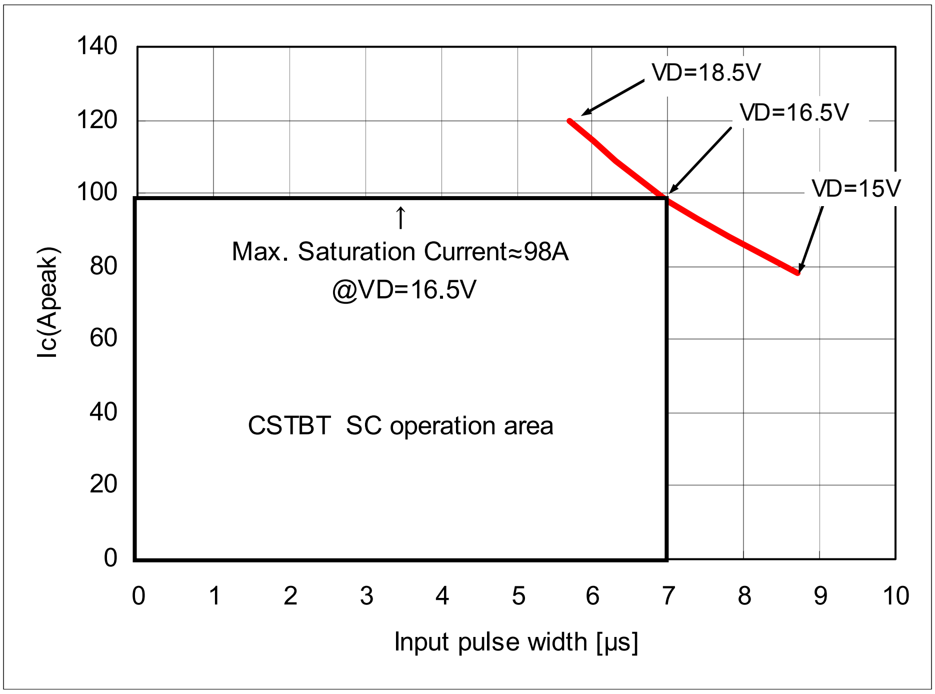


Fig.3-16 PS22A73 typical SCSOA curve

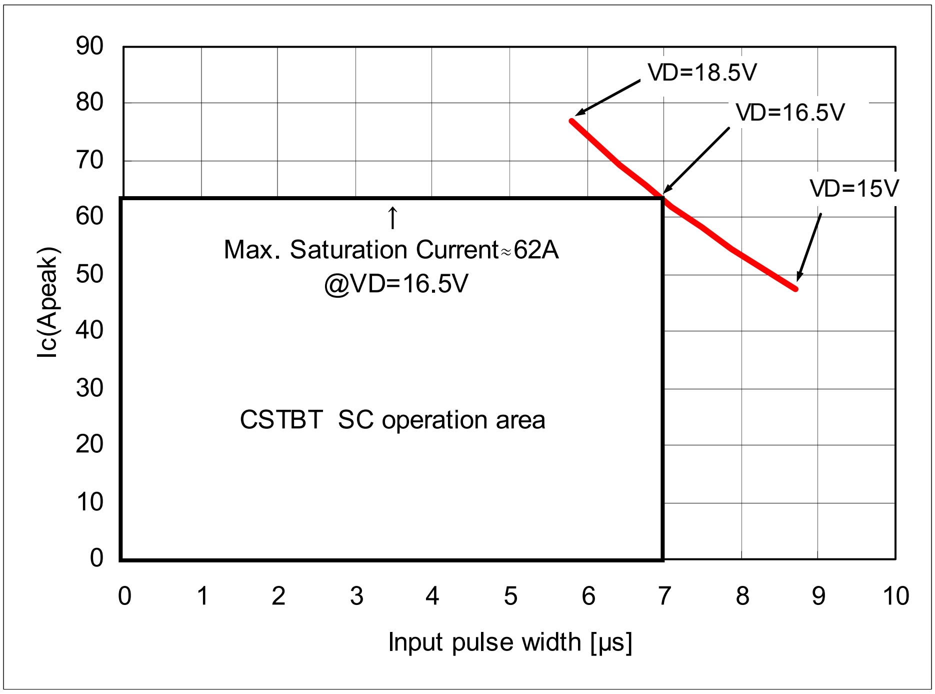


Fig.3-17 PS22A72 typical SCSOA curve

3.1.10 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-18 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).

(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

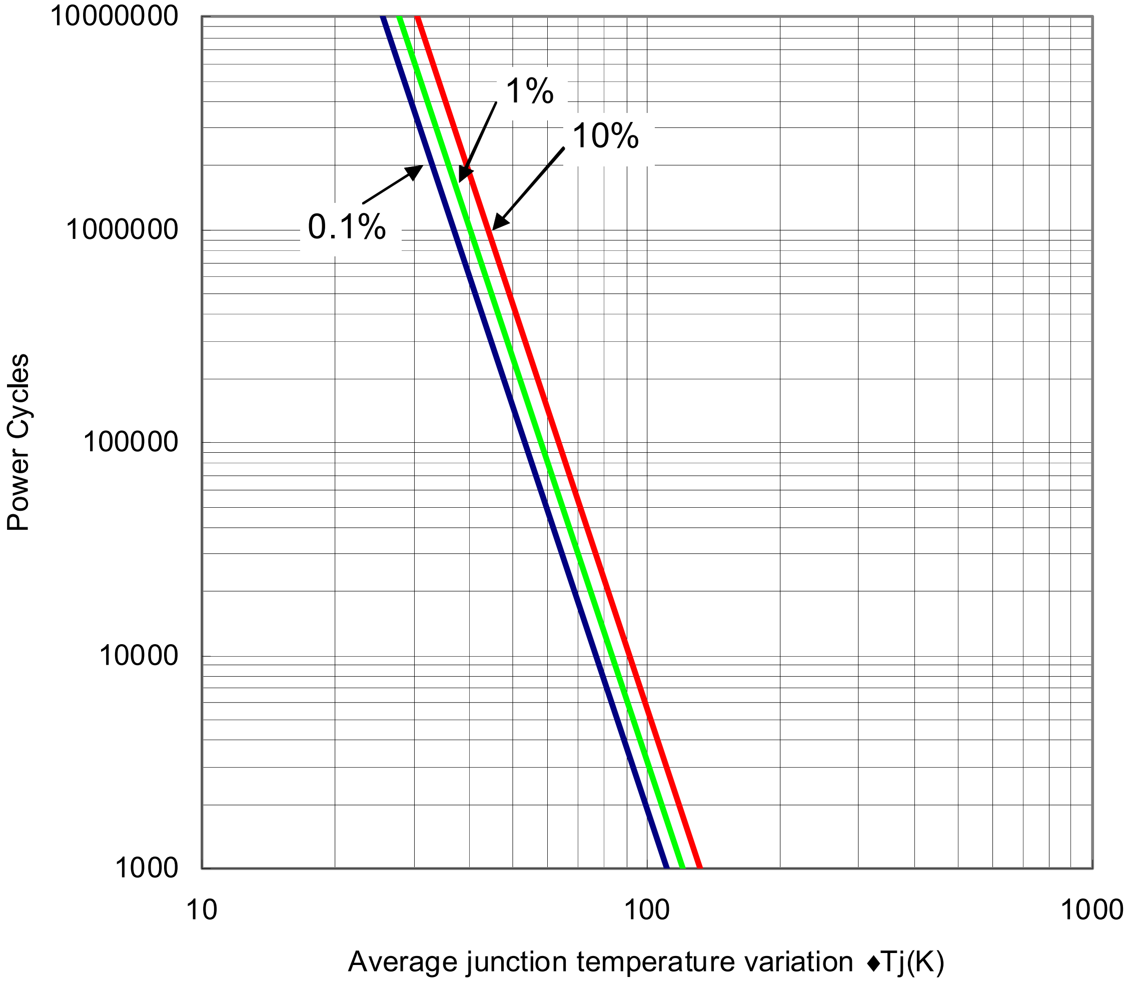


Fig.3-18 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;

(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.

(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).

(4) Output current various with Icp·sinx and it does not include ripple.

(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

- Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin \mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \ \ Duty = \frac{1+D\times\sin(x+\theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\ Icp \times \sin x)$$

$$Vec = (-1)\times Vec(@\ Iecp(=Icp)\times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi}(Icp\times\sin x)\times Vce(sat)(@\ Icp\times\sin x)\times\frac{1+D\sin(x+\theta)}{2}\bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi}((-1)\times Icp\times\sin x)((-1)\times Vec(@\ Icp\times\sin x)\times\frac{1+D\sin(x+\theta)}{2}\bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi}(Psw(on)(@\ Icp\times\sin x)+Psw(off)(@\ Icp\times\sin x))\times fc\bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-19, and its dynamic loss can be calculated by the following expression:

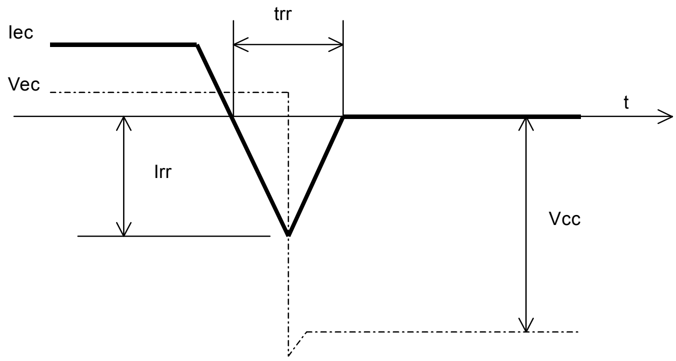


Fig.3-19 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at Tj=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-20 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=600V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., P.F=0.8, Switching loss=Typ., Tj=125°C, Tc=100°C, Rth(j-c)=Max., 3-phase PWM modulation, 60Hz sine waveform output

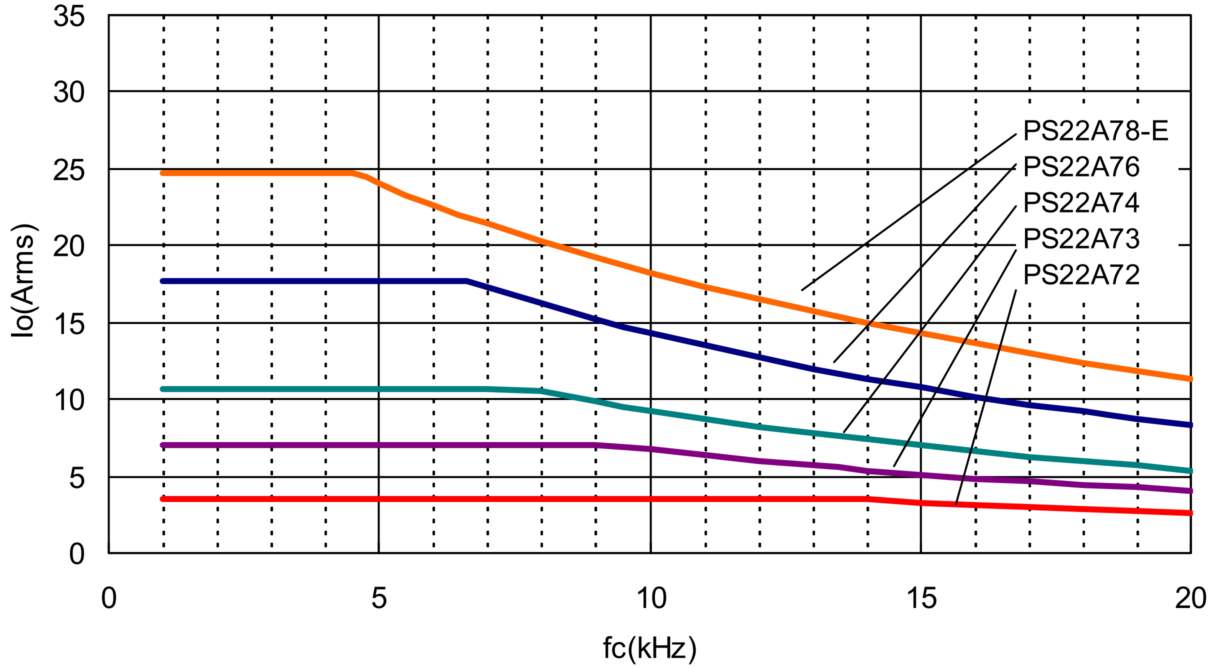


Fig.3-20 Effective current-carrier frequency characteristic

Fig.3-20 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tc=100°C and Tj=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided by Mitsubishi electric on its web site (URL: http://www.mitsubishichips.com/).

3.3 Noise Withstand Capability

3.3.1 Evaluation Circuit

DIPIPM have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-21. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

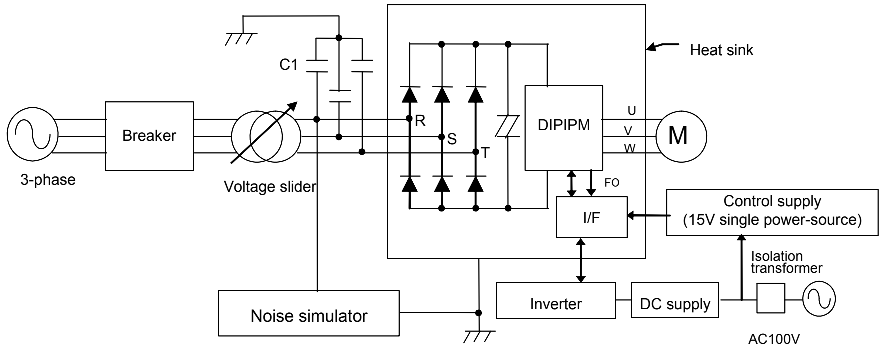


Fig.3-21 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers 15V single power supply, Test is performed with IM

Test conditions

V_{CC}=300V, V_D=15V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

3.3.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

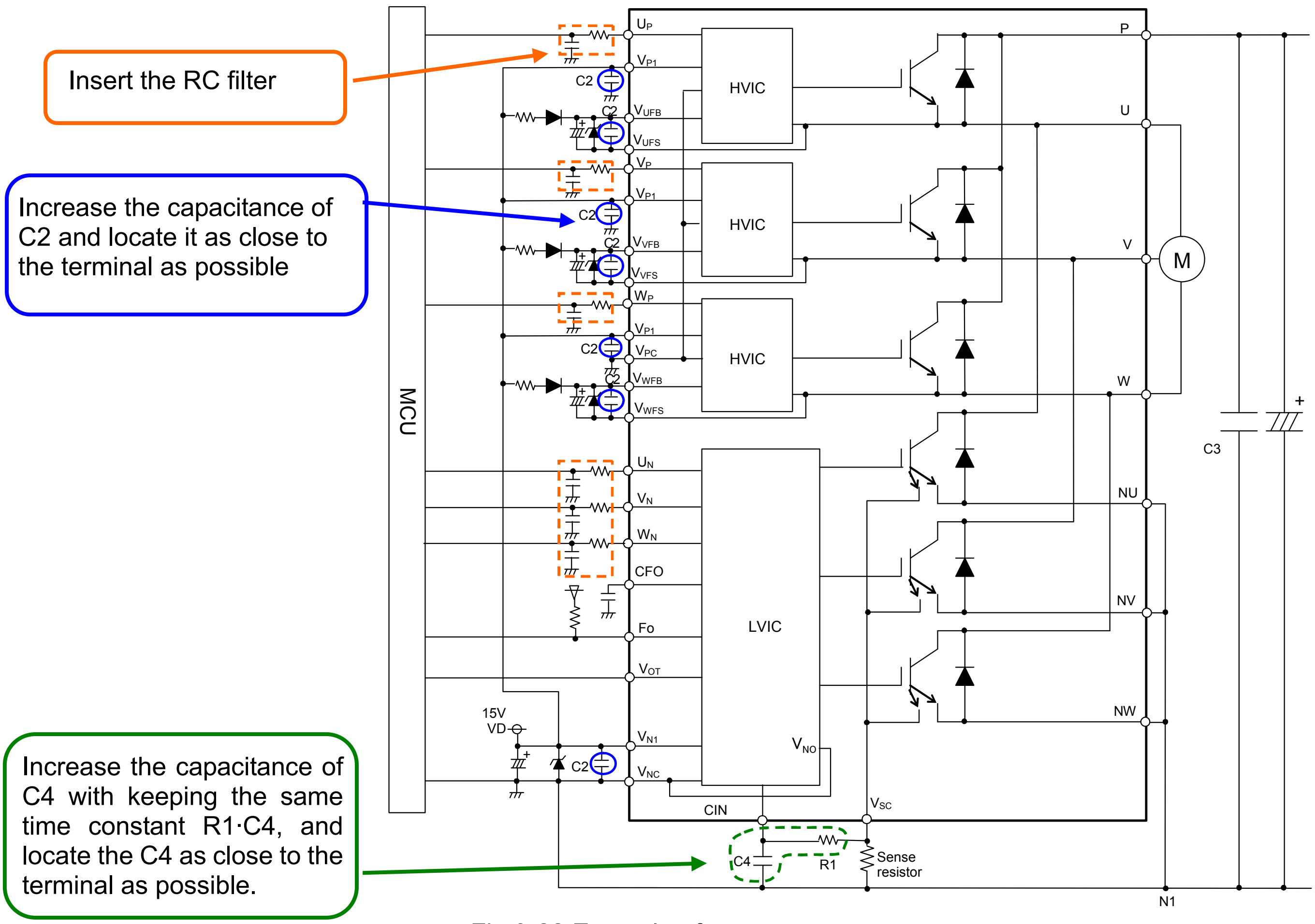


Fig.3-22 Example of countermeasures

3.3.3 Static Electricity Withstand Capability

DIPIPM has been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-23 and Fig.3-24. The results (typical data) are described in Table 3-4

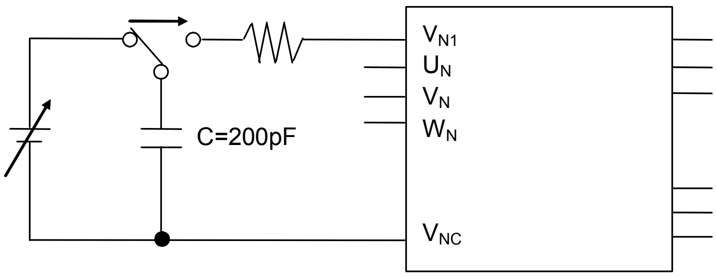


Fig.3-23 V_{N1} terminal Surge Test circuit

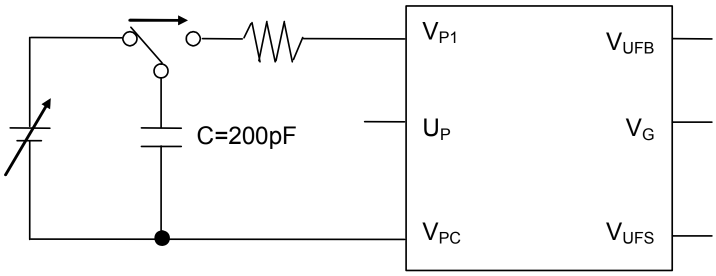


Fig.3-24 V_{P1} terminal Surge Test circuit

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage.
(Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

Table 3-4 Typical ESD capability

[Control terminal part]

For control part, since both have same circuit in the control IC, they have same capability.

Terminals	+	-
UP, VP, WP-V_{NC}	0.7	2.1
V_{P1} - V_{NC}	0.4	2.0
V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	0.5	1.9
UN, VN, WN-V_{NC}	0.8	1.5
V_{N1}-V_{NC}	4.0 or more	4.0 or more
CIN-V_{NC}	0.8	1.4
Fo-V_{NC}	1.6	2.1
CFO-V_{NC}	1.4	1.6
V_{OT}-V_{NC}	1.5	2.0

[Power terminal part for PS22A78-E]

Terminals	+	-
V_{SC}-V_{NC}*	0.3	0.3
P－NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A76]

Terminals	+	-
V_{SC}-V_{NC}*	0.3	0.3
P－NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

* V_{SC} terminal (IGBT sense) is connected to the power chip inside the module.

[Power terminal part for PS22A74]

Terminals	+	-
V_{SC}-V_{NC}*	0.6	0.5
P－NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A73]

Terminals	+	-
V_{SC}-V_{NC}*	0.5	0.5
P－NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A72]

Terminals	+	-
V_{SC}-V_{NC}*	0.5	0.3
P－NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

* V_{SC} terminal (IGBT sense) is connected to the power chip inside the module.

CHAPTER4 KEY PARAMETERS SELECTING GUIDANCE

4.1 Single Supply Drive Scheme

4.1.1 Bootstrap Capacitor Initial Charging

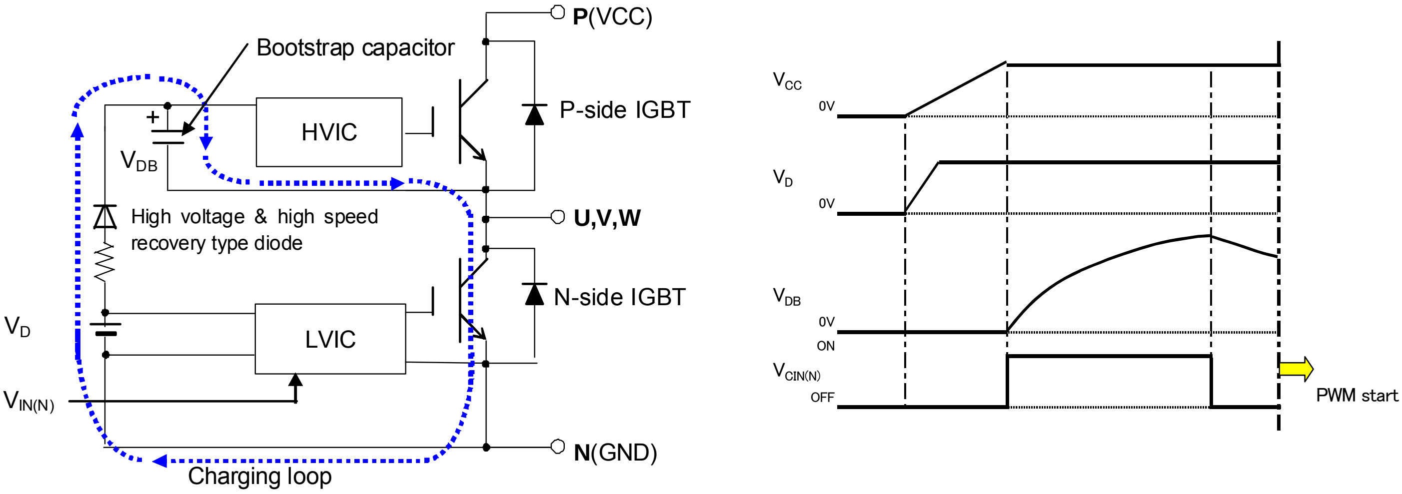


Fig.4-1 Initial charging loop and timing chart of bootstrap circuit

By using bootstrap circuit, conventional three isolated 15V power supply for P-side three IGBT drive can be eliminated. The initial charge of the bootstrap capacitors is necessary to start-up the inverter. Fig.4-2 shows the charge mechanism. The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.

For reference, the charging time for the bootstrap circuit with a 100μF capacitor and 50Ωcurrent limiting resistor is about 5msec.

4.1.2 Charging and Discharging of the Bootstrap Capacitor During Inverter Operation

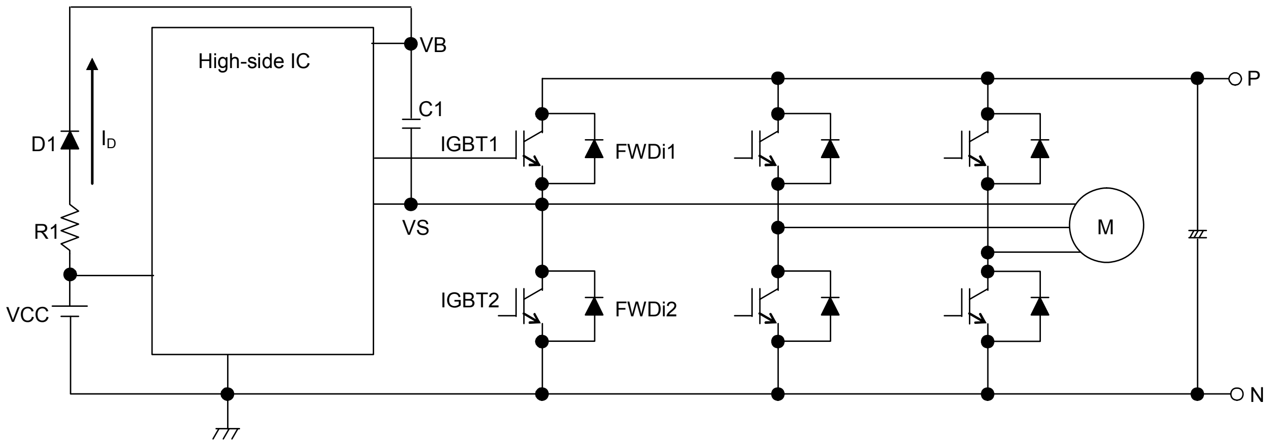


Fig.4-2 Inverter circuit diagram

(1) Charging operation Timing Chart of Bootstrap Capacitor (C1)

Sequence (1-1) : IGBT2 ON (Fig.4-3)

When IGBT2 is in ON state, charging voltage on C1 ($V_{C(1)}$) is calculated by

$V_{C(1)} = V_{CC} - V_{F1} - V_{sat2} - I_D \cdot R1$ (Transient state)

$V_{C(1)} = V_{CC}$ (Steady state)

where V_{CC} is the charging supply voltage, V_{F1} the forward voltage drop of diode D1, V_{sat2} the saturation voltage of IGBT2, I_D the charging current, and R1 the inrush current limitation resistance.

Then, IGBT2 is turned off. Motor current will flow through the free-wheel path of FWDi1. Once the electric potential of VS rises near to that of P, the charging to C1 is stopped.

When IGBT1 is in ON state, the voltage of C1 gradually declines from the potential $V_{C(1)}$ due to the current consumed by the drive circuit.

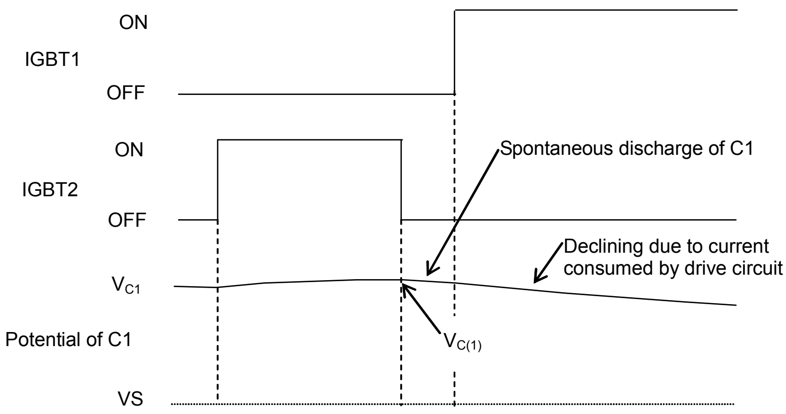


Fig.4-3 Timing chart of sequence (1-1)

Sequence (1-2): IGBT2 OFF and FWDi2 ON (Fig.4-4)
When IGBT2 is OFF and FWDi2 is ON, the voltage on C1 ($V_{C(2)}$) is calculated by:

$$V_{C(2)}=V_{CC}-V_{F1}+V_{EC2}$$

where V_{EC2} denotes the forward voltage drop of FWDi2.

When both IGBT2 and IGBT1 are OFF, the regenerative current flows continuously through the free-wheel path of FWDi2. Therefore the potential of VS drops to $-V_{EC2}$, then C1 is recharged to restore the declined potential. When IGBT1 is turned ON, the potential of V_S rises to that of P, the charge to C1 stops and the voltage on C1 gradually declines from the potential $V_{C(2)}$ due to the current consumed by the drive circuit.

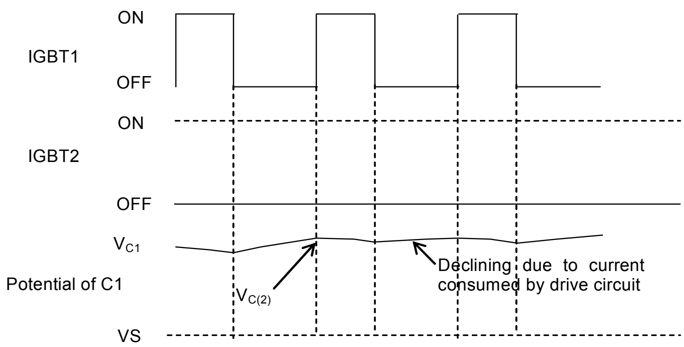


Fig.4-4 Timing chart of sequence (1-2)

（2）Instruction of Selecting the Bootstrap Capacitor (C1) and Resistance (R1)

The capacitance of bootstrap capacitor can be calculated by:

$$C1=I_{BS}\times T1/\Delta V$$

where T1 is the maximum ON pulse width of IGBT1 and I_{BS} is the drive current of the IC (depends on temperature and frequency characteristics), and ΔV is the allowable discharge voltage. A certain margin should be added to the calculated capacitance.

Resistance R1 should be basically selected such that the time constant C1R1 will enable the discharged voltage (ΔV) to be fully charged again within the minimum ON pulse width (T2) of IGBT2.

However, if only IGBT1 has an ON-OFF-ON control mode (Fig.4-5), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

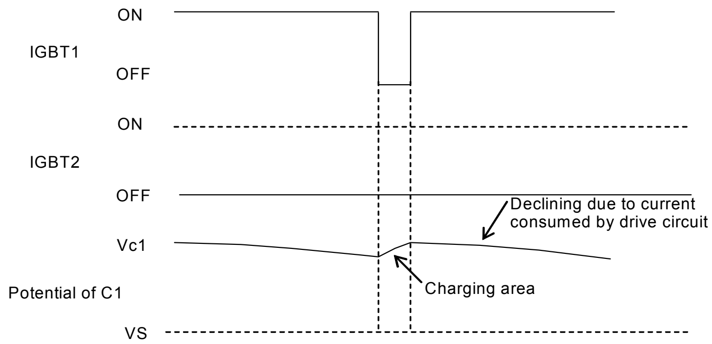


Fig.4-5 Timing Chart of ON-OFF-ON Control Mode

Design example of Bootstrap circuit

■ Selecting bootstrap capacitor

Suppose ΔV_{DB}(discharged voltage)=1V, the maximum ON pulse width T1 of P-side IGBT is 5msec, and I_{DB} is 1.10mA(Max. rating), then

$$C=I_{DB}\times T1/\Delta V_{DB}=5.50\times 10^{-6}$$

the calculated bootstrap capacitance is 5.5μF. By taking consideration of dispersion and reliability, the capacitance is generally selected as large as 2~3 times of the calculated one, for example, 12μF or above for this case is suitable.

■ Selecting bootstrap resistor

Suppose the bootstrap capacitance is 12μF, V_D=15V, V_{DB}=14V, and the minimum ON pulse width t_0 of N-side IGBT (or the minimum OFF pulse width t_0 of upper-side IGBT) is 20μs, then to recover V_{DB} to 15V during this period, the bootstrap resistance should be

$$R=\{(V_D-V_{DB})\times t_0\}/(C\times\Delta V_{DB})\approx 1.7$$

This means a 1.8Ω (selected from E24 series) resistor is suitable.

Note:

(1) In the case of the control for DCBLM or 2-phase modulation for IM (Induction Motor), there will be a long ON time period on the P-side IGBT, please pay attention to the bootstrap supply voltage drop.

(2) The above result is only a calculation example. It is recommended to design a system by taking consideration of the actual control pattern and lifetime of components.

For reference, Fig.4-6 to Fig.4-10 are the circuit current I_{DB} for P-side IGBT driving supply (V_{DB}) vs. carrier frequency characteristics. (@ V_D=V_{DB}=15V, Tj=-20°C (Largest I_{DB} temperature point), IGBT ON Duty=10, 30, 50, 70, 90%)

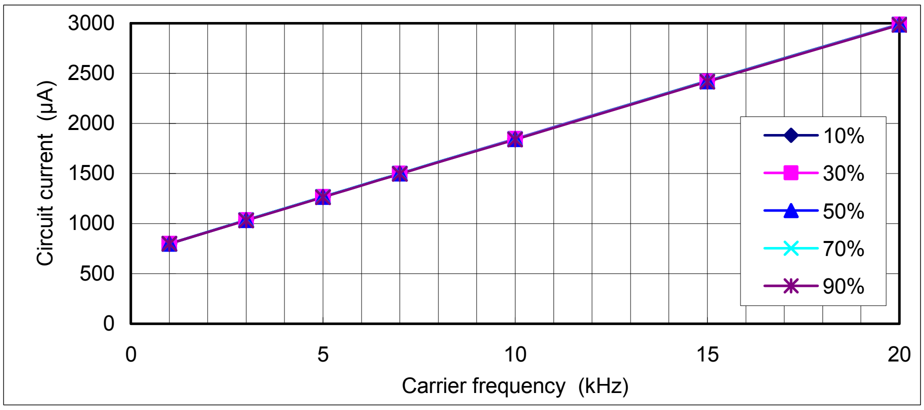


Fig.4-6 I_{DB} vs. Carrier frequency for PS22A78-E

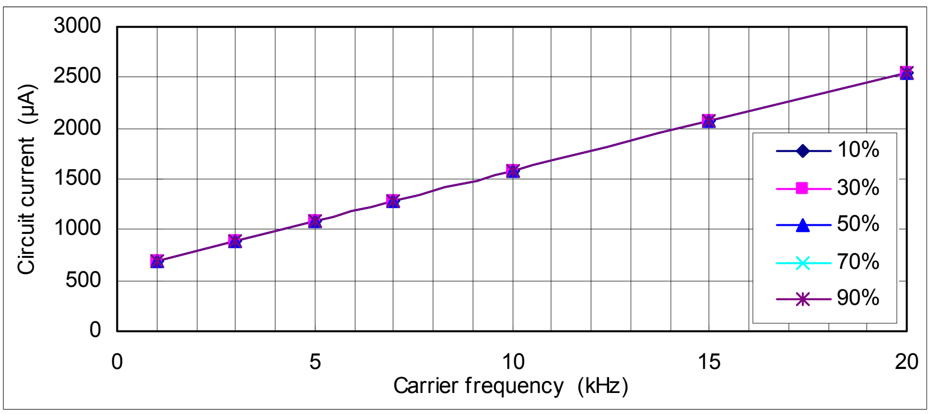


Fig.4-7 I_{DB} vs. Carrier frequency for PS22A76

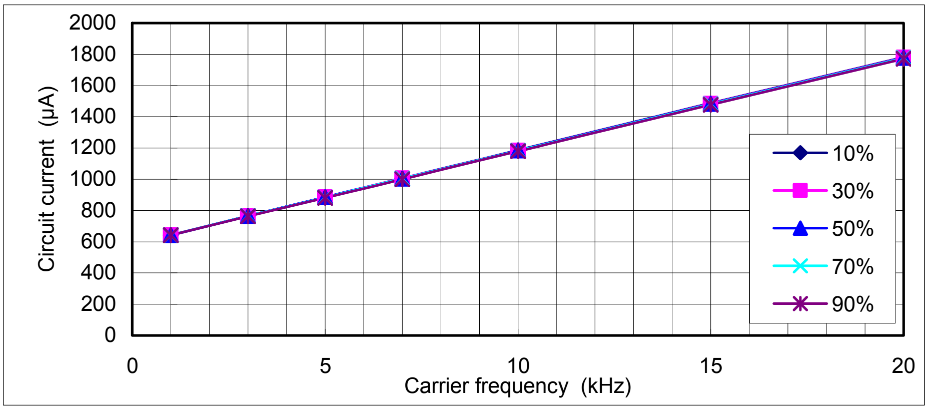


Fig.4-8 I_{DB} vs. Carrier frequency for PS22A74

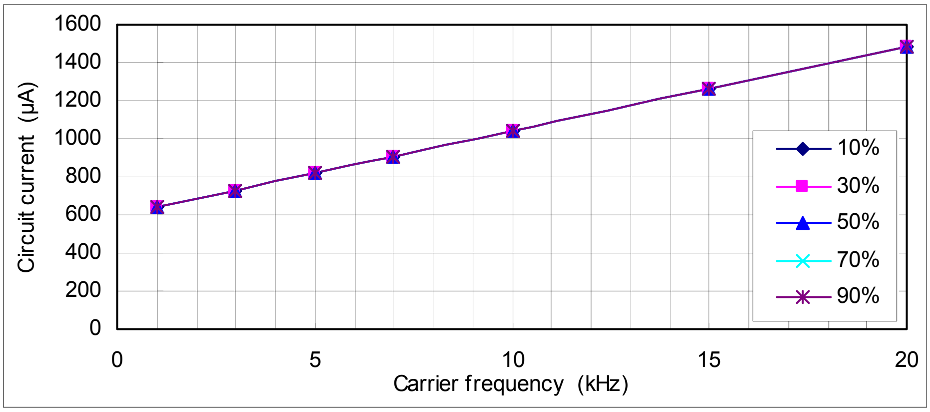


Fig.4-9 I_{DB} vs. Carrier frequency for PS22A73

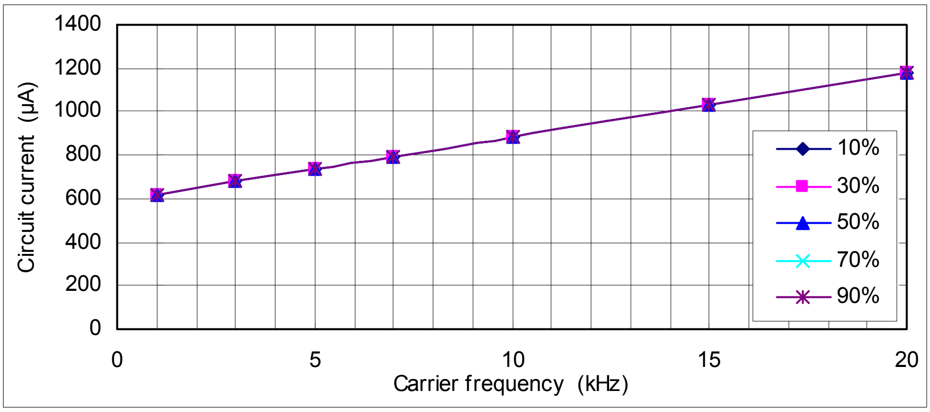


Fig.4-10 I_{DB} vs. Carrier frequency for PS22A72

■ Selecting bootstrap diode

The bootstrap diode with blocking voltage 1200V or more is recommended. In DIPIPM, the maximum rating of power supply is 900V. The actual voltage applied on the diode is 1000V by adding a surge voltage of about 100V. Furthermore, if considering 200V for the margin, 1200V class diode is necessary. The diode is also highly recommended to be with fast recovery characteristics (recovery time less than 100nsec).

■ Noise filter for control supply

It is recommended to insert a 0.22-2μF film or ceramic capacitor for noise filter between the control supply terminals (V_{P1}-V_{NC}, V_{N1}-V_{NC}, V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}). The smaller supply parasitic impedance is, the smaller a feasible noise filter capacitance can be. The supply circuit should be such designed that the noise fluctuation is less than +/-1V/μs, and the ripple voltage is less than +/-2V.

Reference:

There are two kinds of control supply in general use. The first one is DC-DC converter (3-terminal regulator), of which input DC supply comes from AC-transformer. The other is DC-DC converter (switching regulator), of which input DC supply is generated by a SMPS.

Note:

After bootstrap capacitor voltage has been fully charged, input one pulse in the P-side input signals to reset internal IC state before starting formal PWM.

CHAPTER5 PACKAGE HANDLING

5.1 Packaging Specification

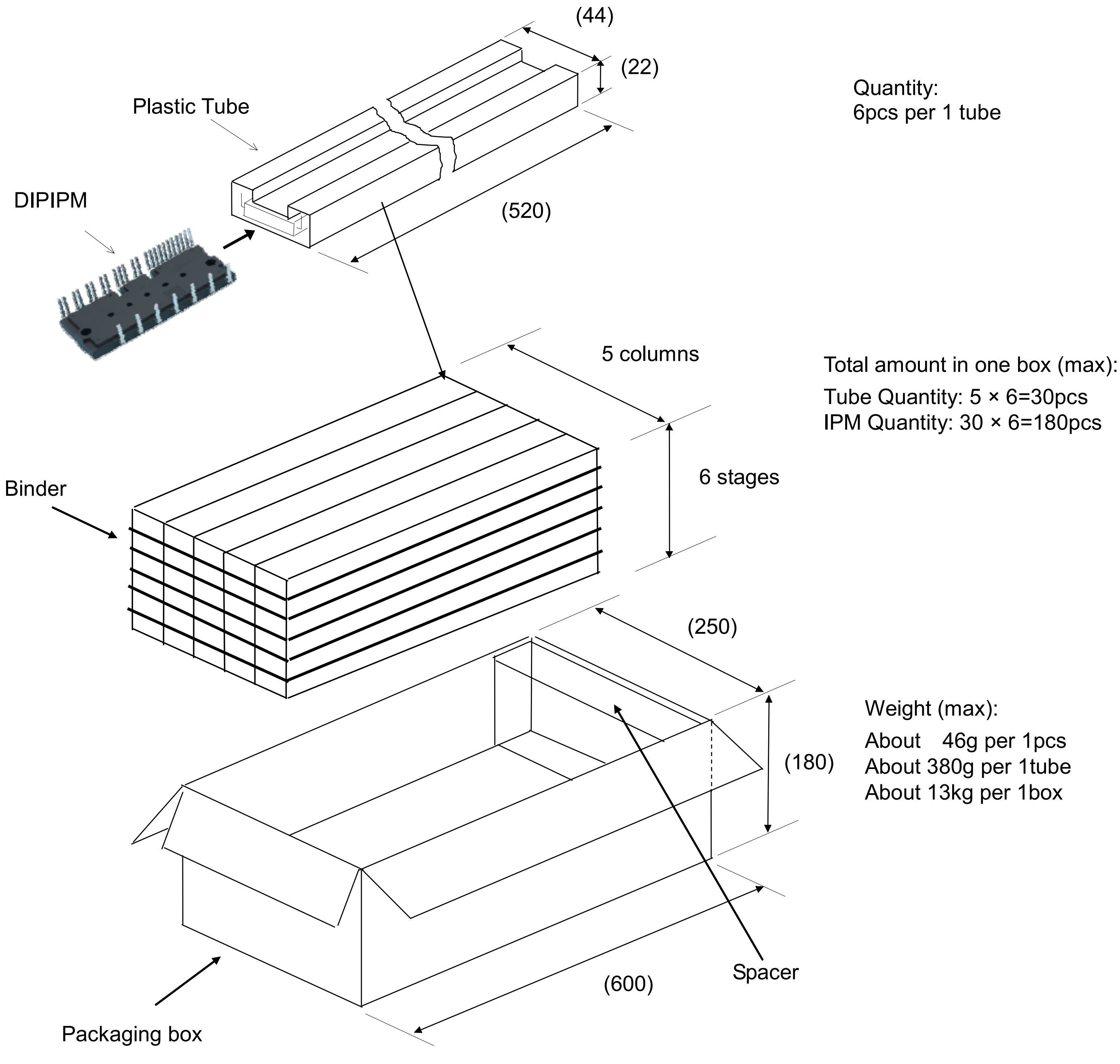


Fig.5-1 Packaging Specification

5.2 Handling Precautions

⚠ Cautions	
Transportation	·Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ·Throwing or dropping the packaging boxes might cause the devices to be damaged. ·Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	·We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	·When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	·Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	·The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	·ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. *Containers that charge static electricity easily should not be used for transit and for storage. *Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. *Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. *During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. *When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. *If using a soldering iron, earth its tip. (2)Notice when the control terminals are open *When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. *Short the terminals before taking a module off.

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Appendix Revision Record

Revision	Page No.	Content
-	-	New